Benefits of Exynos 5420 ISP for Enhanced Imaging Experience

Kisuk Chung, Senior Engineer (kiseok.jeong@samsung.com)
Soyoung Jeong, Assistant Engineer (soy.jeong@samsung.com)
Hyun-Duk Cho, Ph. D. Principal Engineer (hd68.cho@samsung.com)
Hyunkwon Chung, Principal Engineer (hyunkwon.chung@samsung.com)
Kyoungmook Lim, Ph. D. Vice President (km.lim@samsung.com)
System LSI Business
Samsung Electronics
Contents

Abstract 3
Introduction 3
Competitiveness of Exynos 5420 ISP 4
  1. Exynos 5420 ISP Architecture 4
  2. Performance 5
  3. Zero Shutter Lag 5
  4. Low Preview Power Consumption 6
  5. Image Quality Enhancement Features 6
  6. Computational Photography 6
Summary 7
References 8
Abstract

Exynos 5 Octa includes an internal Image Signal Processor (ISP), which can process a single 13 MP 30 fps, or 24 MP 16 fps Bayer image stream. It supports zero shutter lag at 30 fps performance domain in addition to multiple image enhancement features with low power consumption. Additionally, it also includes add-on hardwired post-processing units, which enhance the image quality, such as:

- Dynamic Range Compensation (DRC)
- Video Digital Image Stabilization (VDIS)
- 3-Dimensional Noise Reduction (3DNR)
- Face Detection (FD)

Exynos 5420 ISP also offers optimized hardware for implementation of computational photography applications with powerful CPU and GPU. This paper, discusses multiple key advantages and competitiveness of Exynos 5420 ISP over other ISPs in terms of performance, advanced features and low power consumption.

Introduction

Mobile device users carry their devices everywhere. Hence, they can click photos and easily share them by using Social Network Service (SNS). It has become an essential part of today’s life. This culture is reshaping our daily lives and mobile users expect better user experience, which is a byproduct of better image quality. This can be achieved by implementing state-of-the-art image processing techniques.

Today’s smartphone cameras are improved to satisfy the growing user expectation. Thanks to the ever increasing resolution, and fidelity of the mobile camera lens and sensor, nowadays, smartphones have also stepped into the digital camera space. Additionally, smartphones enable the user to apply special effects on the photos, by using some filters or computational photography.

Due to these reasons, the image processing capability of smartphones which mainly affects camera performance is gaining importance. Today, it is one of the crucial points for smartphone manufacturers to gain the competitive edge in the industry.

ISP performs image processing to enhance the image quality of the photograph and features in mobile Application Processor (AP). Its primary function is to enhance the quality of raw Bayer images that a CMOS image sensor takes from the real world. The enhancement is done before performing additional functions, such as color space conversion and image scaling.

Earlier, almost all smartphones included a stand-alone ISP, in addition to mobile AP. This is because of the low performance and poor image quality of the internal ISP even in smartphone cameras. However, currently there is no reason to use other discrete chips in smartphones for image processing. This is because of the powerful internal ISPs in mobile AP, such as Exynos 5420. It can support a high
mega pixel resolution of 13 MP 30 fps, in addition to various image quality enhancement features, known as post-processing. Additionally, it also includes a camera 2.0 path for computational photography with low power consumption. The next section, describes details about Exynos 5420 ISP.

### Competitiveness of Exynos 5420 ISP

#### 1. Exynos 5420 ISP Architecture

Exynos 5420 includes an internal ISP to process single Bayer image stream with 13 MP 30 fps or, 24 MP 16 fps. ISP converts Bayer format image to YUV format, and also manages video preview/camcording along with image capture. Additionally, Exynos 5420 ISP can also perform a variety of major signal processing functions such as:

- Sensor defect compensation
- 3A statistics gathering
- Demosaicing
- Denoising

As illustrated in figure 3, Exynos 5420 ISP comprises:

- Sequential connection of sub-IPs which includes the core ISP block
- Image enhancements IPs such as DRC, VDIS, 3DNR, FD
- Scaler for resizing of images

You can select the input/output images of each sub-IP from/to the on-the-fly, or DMA path. For example, you can select the Bayer format input image of the core ISP block either from on-the-fly or through DMA. The output image of the core ISP block can be selected to either on-the-fly or DMA.

Image quality enhancement block, is known as the post-processor. It consists of multiple sub-IPs. DRC applies an adaptive tone mapping curve to each pixel of the input image data for better dynamic range. VDIS stabilizes the input video to compensate shaking of the hand. 3DNR is used for inter-frame noise reduction, and FD detects the face which is to be focused. Refer to section 5 for more information on image quality enhancement blocks.
2. Performance

Nowadays, high standards of image quality and processing performance is required for ISP design. Exynos 5420 includes a remarkable ISP for the best image quality and the fastest processing speed in image and video.

Exynos 5420 ISP can support as high pixel throughput as 450 MP/s. More specifically, it can process up to 13 MP and 2 MP 14-bit Bayer RGB format with 30 fps simultaneously. One of the primary advantages of using this dual camera support case is that it supports full-HD dual camcording, known as Picture in Picture (PIP). It combines a 13 MP rear Bayer input and 2 MP front Bayer input into a single full-HD (2 MP) video stream, as illustrated in figure 4.

![Full-HD PIP Support](image)

**Figure 4: Full-HD PIP Support**

Exynos 5420 ISP also supports burst still capture mode up to 13 MP 12 fps without shutter lag issues. This is one of the primary advantages of Exynos 5420 over its predecessors (Exynos 4412 and Exynos 5250) and other internal ISPs. Exynos 5420 ISP provides a better performance than Exynos 4412 and 5250 by x3.8 and x1.9 respectively in terms of pixel throughput, as illustrated in figure 5.

![Exynos ISP Performance](image)

**Figure 5: Exynos ISP Performance**

3. Zero Shutter Lag

One of the common issues that users face in many mobile devices and digital still cameras is the time lag between clicking a photo and actual capturing of the image by the camera. It is known as shutter lag problem. As illustrated in figure 6, an user clicks the shot button to capture red image in T₀ time-frame, but there is no Bayer dump path to buffer preview Bayer stream. Therefore, the user has no choice but to get the blue image which is in T₃ time-frame. That is to say, the user cannot help getting the frame delayed image.

![Shutter Lag Problem in Common Devices](image)

**Figure 6: Shutter Lag Problem in Common Devices**

To capture the exact moment without any shutter lag, ISP should ensure that the incoming Bayer data from the sensor is retained, and should pull it when a shutter button is clicked while displaying preview data on the screen. For this reason, Exynos 5420 ISP dumps incoming 13 MP Bayer images into the frame buffer all the time during the preview mode for image capture.

Figure 7 illustrates the zero shutter lag of Exynos 5420 ISP. This indicates that the user does not experience any shutter lag. As illustrated in figure 7, the user requires to click the shot button to capture the red image in T₀ time-frame. Later, the user receives the similar red image in T₀ time-frame without any frame delay. This is because the still image data from the Bayer input is dumped on the frame buffer.

![Zero Shutter Lag Support in Exynos 5420 ISP](image)

**Figure 7: Zero Shutter Lag Support in Exynos 5420 ISP**
4. Low Preview Power Consumption

For low power consumption in preview and camcording mode, Exynos 5420 ISP implements advanced architecture. In comparison to the conventional architecture, Exynos 5420 ISP consumes 35% less power in full-HD 30 fps single preview mode. Conventional ISP architecture processes preview images in full resolution, as illustrated in figure 8. For example, in case of a 13 MP CIS, conventional ISP processes 13 MP Bayer images at 30 fps even in preview mode, where full-HD resolution is good enough. This full resolution preview consumes high power. This is because, it requires very high operation frequency.

Figure 8: Preview Processing in Conventional ISP

To reduce power consumption during preview, Exynos 5420 includes a power optimization logic to scale down the preview image from 13 MP to 3 MP, as illustrated in figure 9. The logic enables Exynos 5420 ISP to reduce full-HD 30 fps preview power consumption by about 35% over conventional ISP. Additionally, it also enhances the battery life.

Figure 9: Preview Processing in Exynos 5420 ISP

5. Image Quality Enhancement Features

Exynos 5420 ISP supports these image quality enhancement features such as DRC, ODC, VDIS, 3DNR and FD that hardwired IPs provide, as illustrated in figure 10.

DRC adjusts the dynamic range, which results in images that are either too dark or too bright. Therefore, DRC feature lightens the heavily dark parts, or dims the intensely bright parts. The DRC of Exynos 5420 ISP adaptively generates a tone mapping curve and applies a tone curve to each pixel of the input image data. The strength, asymmetry, slope limit and amplification limit control the shape of the curve. DRC also supports non-linear color correction function for enhanced regions and preservation of local contrast.

VDIS controls image stability and reduces the effects of camera shake caused by hand jingle or external environment. Additionally, it compensates for the blurred shaky video. The VDIS of Exynos 5420 ISP differentiates unwanted camera or object motion from the intentional camera motion. It can detect translational movements such as forward/back, left/right and up/down and rotational movements such as roll, pitch and yaw. The input image resolution for VDIS is 3 MP. After VDIS processing, the size of the output image is scaled down to 2 MP (full-HD), in order to fit with the final size of the image sequence to be recorded.

3DNR feature reduces the visible noise in the video footage. It can distinguish and remove noise from the useful details by analyzing neighboring frames in the video stream. This is because there is a high correlation between the pixels of same position in sequential frames. The 3DNR block of Exynos 5420 ISP should be located after VDIS block. This is because any unwanted motion in the video due to hand movement, results in a motion blur artifact in the processed frame. 3DNR supports up to full-HD 60 fps video input resolution along with YUV422 8-bit format.

The hardware and software implement the FD features of Exynos 5420 ISP. Most calculations are done by the software, but the hardware pre-computes some data for software use. The hardware pre-computes data maps on-the-fly and writes them to memory. Then the software accesses pre-computed maps and performs actual classification to detect faces and tracking. By pre-computing data with a hardware accelerator, 2 times speed-up of total time can be achieved. Additionally, FD library can be tuned further to achieve required performance and detection ratio.

6. Computational Photography

Exynos 5420 ISP offers optimized hardware to implement computational photography. The required functions in the hardware ISP pipeline can be bypassed, so software applications easily replace hardware functions. The Bayer image data from the image sensor can be sent directly to the CPU or GPU, allowing applications to perform their own processing, or store the Bayer data for future...
processing. In the mean time, ISP can get the Bayer image back from the CPU or GPU, so it can be further processed in the ISP pipeline.

Figure 11: Example of Computational Photography Support in Exynos 5420

Computational photography requires these key features, which Exynos 5420 offers:

- Bypassing of the hardware processing block
- Accessing of raw image data by CPU or GPU
- Reinjecting of raw image data into the hardware processing block
- Powerful CPU and GPU to perform image processing computation
- High memory bandwidth for reading and writing large amounts of data

Exynos 5420 ISP completely supports the demanding requirements of computational photography. This allows the execution of a variety of advanced photographic applications on mobile devices, resulting in enhanced user experience.

Summary

This paper describes the performance of Exynos 5420 internal ISP, and advanced power enhancement features in comparison to the predecessor ISPs. Exynos 5420 ISP provides a higher performance competitiveness than ISPs of Exynos 4412 and Exynos 5250 by x3.8 and x1.9 respectively in terms of pixel throughput. To reduce the preview power consumption, Exynos 5420 includes a power optimization logic. It can reduce the preview power consumption in full-HD 30fps by about 35% over conventional ISPs.

This paper also describes several image quality enhancement features. Exynos 5420 ISP includes hardwired post processors, such as DRC, VDIS, 3DNR and FD. These features provide performance and power competitiveness over software solution based ISPs.

Finally, the paper also describes the benefits of computational photography support. Exynos 5420 ISP offers optimized hardware. This allows photographic applications that are executed on mobile devices to offer the best experience for the end users.
References

About Samsung Electronics Co., Ltd.

Samsung Electronics Co., Ltd. is a global leader in technology, opening new possibilities for people everywhere. Through relentless innovation and discovery, we are transforming the worlds of televisions, smartphones, personal computers, printers, cameras, home appliances, LTE systems, medical devices, semiconductors and LED solutions. We employ 236,000 people across 79 countries with annual sales exceeding US$187.8 billion. To discover more, please visit [www.samsung.com](http://www.samsung.com).

For more information


For more information about Samsung Exynos Processor, visit

[http://www.exynos.com](http://www.exynos.com)


[http://twitter.com/SamsungExynos](http://twitter.com/SamsungExynos)

[http://youtube.com/SamsungExynos](http://youtube.com/SamsungExynos)

Copyright © 2013 Samsung Electronics Co. Ltd. All rights reserved. Samsung is a registered trademark of Samsung Electronics Co. Ltd. Specifications and designs are subject to change without notice. Non-metric weights and measurements are approximate. All data were deemed correct at time of creation. Samsung is not liable for errors or omissions. All brand, product, service names and logos are trademarks and/or registered trademarks of their respective owners and are hereby recognized and acknowledged.

Samsung Electronics Co., Ltd.
416, Maetan 3-dong,
Yeongtong-gu
Suwon-si, Gyeonggi-do 443-772,
Korea

[www.samsung.com](http://www.samsung.com)