

# Async(Low Power) SRAM Code Information(1/4)

**K 6 X X X X X X X X - X X X X X X X**  
 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

## 1. Memory (K)

2. Async (Low Power) SRAM : 6

## 3. Small Classification

C : CellularRAM  
 E : Corner Vcc/ Vss + Fast SRAM  
 F : fCMOS Cell + Low Power SRAM  
 H : High Speed (Low Power SRAM)  
 X : High Voltage (Low Power SRAM)  
 J : BICMOS  
 R : Center Vcc/Vss + Fast SRAM  
 S : EMLSI Async SRAM  
 T : TFT Cell + SPSRAM  
 M : Mobile SRAM

## 4~5. Density

06 : 64K	08 : 256K	09 : 512K
10 : 1M	12 : 512M	16 : 16M
20 : 2M	28 : 128M	30 : 3M
32 : 32M	40 : 4M	56 : 256M
64 : 64M	80 : 8M	1G : 1G

## 6~7. Organization

04 : x4	08 : x8
16 : x16	24 : x24

## 8. Vcc

C : 5.0V	Q : 3.0V (VDDQ=1.8V)
R : 1.65V~2.2V	S : 2.5V
T : 2.7V~3.6V	U : 3.0V
V : 3.3V	W : 2.2V~3.3V

## 9. Mode

1 : CS Low Active  
 2 : CS1, CS2 - Dual Chip Select Signal  
 3 : Single Chip Select with /LB, /UB (tOE)  
 4 : Single Chip Select with /LB, /UB (tCS)  
 6 : Dual Chip Select with /LB, /UB (tCS)  
 7 : I/Os Control with /BYTE  
 9 : Multiplexed Address  
 A : Mirror Chip Option  
 B : Page Mode  
 C : Sync. Burst

## 10. Generation

M : 1st Generation  
 A : 2nd Generation  
 B : 3rd Generation  
 C : 4th Generation  
 D : 5th Generation  
 E : 6th Generation  
 F : 7th Generation  
 G : 8th Generation  
 H : 9th Generation

## 11. "—"

## 12. Package

A : TBGA (Lead-Free)	B : SOP (Lead-Free)
C : CHIP BIZ	D : DIP
E : TBGA	F : FBGA
G : SOP	H : BGA
J : SOJ	K : SOJ (Lead-Free)
L : TSOP1-0813.4 (Lead-Free)	
P : TSOP1-0820 (Lead-Free)	
Q : TSOP2-400R (Lead-Free)	R : TSOP-R
T : TSOP	
U : TSOP2-400 (Lead-Free)	
W : WAFER	X : FBGA (Lead-Free)

# Async(Low Power) SRAM Code Information(2/4)

**K** **6** X X X X X X X X - X X X X X X
  
 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

※ **Exception**

- 512K/1M/2M/4M Low Power SRAM

- 32-TSOP1-0813.4F → **Y**
- 32-TSOP1-0813.4 → **Y**
- 32-TSOP1-0813.4R → **N**

- 4M Low Power SRAM

- 32-TSOP2-400F → **V**
- 32-TSOP2-400R → **M**

**13. Temp, Power**

- COMMON (Temp, Power)

- A : Automotive, Normal
- B : Commercial, Low Low
- C : Commercial, Normal
- D : Extended, Low Low
- E : Extended, Normal
- F : Industrial, Low Low
- I : Industrial, Normal
- L : Commercial, Low
- P : Industrial, Low
- Q : Automotive, Low
- R : Industrial, Super Low
- 0 : NONE, NONE

- WAFER,CHIP BIZ Level Division

- 0 : NONE, NONE
- 1 : Hot DC sort
- 2 : Hot DC, selected AC sort
- 3 : Cold/Hot DC, selected AC sort

**14~15. Speed (tAA)**

- fCMOS Cell + Low Power SRAM

- |            |            |
|------------|------------|
| 10 : 100ns | 12 : 120ns |
| 25 : 25ns  | 35 : 35ns  |
| 45 : 45ns  | 55 : 55ns  |
| 70 : 70ns  | 85 : 85ns  |
- DS : Daisychain Sample

- TFT Cell + Low Power SRAM

- |            |            |
|------------|------------|
| 10 : 100ns | 12 : 120ns |
| 35 : 35ns  | 45 : 45ns  |
| 55 : 55ns  | 70 : 70ns  |
| 85 : 85ns  |            |
- DS : Daisychain Sample

- High Speed (Low Power SRAM)

- |           |           |
|-----------|-----------|
| 20 : 20ns | 25 : 25ns |
|-----------|-----------|

- High Voltage (Low Power SRAM)

- |           |           |           |
|-----------|-----------|-----------|
| 55 : 55ns | 70 : 70ns | 85 : 85ns |
|-----------|-----------|-----------|

- Corner Vcc/Vss + Fast SRAM

- |           |           |           |
|-----------|-----------|-----------|
| 10 : 10ns | 12 : 12ns | 15 : 15ns |
|-----------|-----------|-----------|

- BICMOS

- |           |           |           |
|-----------|-----------|-----------|
| 08 : 8ns  | 09 : 9ns  | 10 : 10ns |
| 12 : 12ns | 15 : 15ns | 20 : 20ns |
- 8A : 8.6ns

- Center Vcc/Vss + Fast SRAM

- |           |           |           |
|-----------|-----------|-----------|
| 08 : 8ns  | 09 : 9ns  | 10 : 10ns |
| 12 : 12ns | 15 : 15ns | 20 : 20ns |

# Async(Low Power) SRAM Code Information(3/4)

<u>K</u>	<u>6</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>-</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17 18

- Mobile SRAM

55 : 55ns	70 : 70ns
85 : 85ns	
B1 : 66MHz/70ns	B2 : 66MHz/55ns
B3 : 66MHz/45ns	B4 : 66MHz/35ns
C1 : 80MHz/70ns	C2 : 80MHz/55ns
C3 : 80MHz/45ns	C4 : 80MHz/35ns
D1 : 104MHz/70ns	D2 : 104MHz/55ns
D3 : 104MHz/45ns	D4 : 104MHz/35ns
E1 : 133MHz/70ns	E2 : 133MHz/55ns
E3 : 133MHz/45ns	E4 : 133MHz/35ns

- CellularRAM

55 : 55ns	70 : 70ns
85 : 85ns	
B1 : 66MHz/70ns	B2 : 66MHz/55ns
B3 : 66MHz/45ns	B4 : 66MHz/35ns
C1 : 80MHz/70ns	C2 : 80MHz/55ns
C3 : 80MHz/45ns	C4 : 80MHz/35ns
D1 : 104MHz/70ns	D2 : 104MHz/55ns
D3 : 104MHz/45ns	D4 : 104MHz/35ns
E1 : 133MHz/70ns	E2 : 133MHz/55ns
E3 : 133MHz/45ns	E4 : 133MHz/35ns

- Async SRAM COMMON

00 : NONE  
(Containing Wafer, CHIP BIZ, Exception code)

# Async(Low Power) SRAM Code Information(4/4)

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## 16. Packing Type

- Common to all products, except of Mask ROM
- Divided into TAPE & REEL(In Mask ROM, divided into TRAY, AMMO Packing Separately)

Divide	Packing Type	New Marking
<b>Component</b>	TAPE & REEL	T
	Other ( Tray, Tube, Jar )	0 ( Number)
	Stack	S
<b>Module</b>	MODULE TAPE & REEL	P
	MODULE Other Packing	M

## 17~18. Customer "Customer List Reference"