

DDR2 Code Information(1/2)

Last Updated : November 2008

K	4	T	X	X	X	X	X	X	X	-	X	X	X	X	X	X	
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

1. Memory (K)

2. DRAM : 4

3. Small Classification

T : DDR2 SDRAM

4~5. Density

51 : 512M

56 : 256M

1G : 1G

2G : 2G

4G : 4G

6~7. Bit Organization

04 : x4

06 : x4 Stack

07 : x8 Stack

08 : x8

16 : x16

26 : x4 Stack (JEDEC Standard)

27 : x8 Stack (JEDEC Standard)

8. # of Internal Banks

3 : 4Bank

4 : 8Bank

9. Interface, VDD, VDDQ

Q : SSTL, 1.8V, 1.8V

10. Generation

11. "-"

12. Package

Z : FBGA (Lead-Free)

J : FBGA (Lead-Free, DDP)

Q : FBGA (Lead-Free, QDP)

H : FBGA (Lead-Free, Halogen-Free)

M : FBGA (Lead-Free, Halogen-Free, DDP)

T : FBGA (Lead-Free, Halogen-Free, QDP)

13. Temp, Power

C : Commercial, Normal

L : Commercial, Low

Y : Commercial, Low Voltage

14~15. Speed (Wafer/Chip Biz/BGD: 00)

CC : DDR2-400 (200Mhz@CL=3, tRCD=3, tRP=3)

D5 : DDR2-533 (266Mhz@CL=4, tRCD=4, tRP=4)

E6 : DDR2-667 (333Mhz@CL=5, tRCD=5, tRP=5)

F7 : DDR2-800 (400Mhz@CL=6, tRCD=6, tRP=6)

E7 : DDR2-800 (400Mhz@CL=5, tRCD=5, tRP=5)

DDR2 Code Information(2/2)

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<u>K</u>	<u>4</u>	<u>T</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>-</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

16. Packing "Packing Type Reference"

- Common to all products, except of Mask ROM
- Divided into TAPE & REEL(In Mask ROM, divided into TRAY, AMMO Packing Separately)

Divide	Packing Type	New Marking
Component	TAPE & REEL	T
	Other (Tray, Tube, Jar)	0 (Number)
	Stack	S
Module	MODULE TAPE & REEL	P
	MODULE Other Packing	M

17~18. Customer "Customer List Reference"