

DDR3 Code Information(1/2)

Last Updated : November 2008

<u>K</u>	<u>4</u>	<u>B</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>-</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

1. Memory (K)

2. DRAM : 4

3. Small Classification

B : DDR3 SDRAM

4~5. Density

1G : 1G

2G : 2G

4G : 4G

6~7. Bit Organization

04 : x4

08 : x8

16 : x16

8. # of Internal Banks

4 : 8 Banks

9. Interface, VDD, VDDQ

6 : SSTL, 1.5V, 1.5V

10. Generation

11. "—"

12. Package

Z : FBGA (Lead-Free)

H : FBGA (Halogen-free & Lead-Free)

J : FBGA (Lead-Free, DDP)

M : FBGA (Halogen-Free & Lead-Free, DDP)

13. Temp, Power

C : Commercial Temp.(0°C ~ 85°C), Normal Power

L : Commercial Temp.(0°C ~ 85°C), Low Power

14~15. Speed (Wafer/Chip Biz/BGD: 00)

F7 : DDR3-800 (400Mhz@CL=6, tRCD=6, tRP=6)

F8 : DDR3-1066 (533MHz@CL=7, tRCD=7, tRP=7)

H9 : DDR3-1333 (667MHz@CL=9, tRCD=9, tRP=9)

K0 : DDR3-1600 (800MHz@CL=11, tRCD=11, tRP=11)

DDR3 Code Information(2/2)

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1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

16. Packing "Packing Type Reference"

- Common to all products, except of Mask ROM
- Divided into TAPE & REEL(In Mask ROM, divided into TRAY, AMMO Packing Separately)

Divide	Packing Type	New Marking
Component	TAPE & REEL	T
	Other (Tray, Tube, Jar)	0 (Number)
	Stack	S
Module	MODULE TAPE & REEL	P
	MODULE Other Packing	M

17~18. Customer "Customer List Reference"