

DDR SDRAM Code Information(1/2)

Last Updated : May 2008

K **4** X X X X X X X X - X X X X X X X
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

1. Memory (K)

2. DRAM : 4

3. Small Classification

H : DDR SDRAM

4~5. Density, Refresh

64 : 64Mb, 4K/64ms
28 : 128Mb, 4K/64ms
51 : 512Mb, 8K/64ms
56 : 256Mb, 8K/64ms
1G : 1Gb, 8K/64ms
2G : 2Gb, 8K/64ms

6~7. Organization

04 : x4
08 : x8
16 : x16
32 : x32
06 : x4 Stack
07 : x8 Stack

8. Bank

3 : 4Bank

9. Interface, VDD, VDDQ

8 : SSTL-2, 2.5V, 2.5V

10. Generation

11. "-"

12. Package

T : TSOP2
U : TSOP2 (Lead Free)
L : TSOP2 (Lead-Free & Halogen-Free)
N : sTSOP2
V : sTSOP2 (Lead Free)
6 : sTSOP2 (Lead-Free & Halogen-Free)
G : FBGA
Z : FBGA (Lead Free)
H : FBGA (Lead-Free & Halogen-Free)
F : FBGA for DDR 64Mb/128Mb
(Lead-Free & Halogen-Free)

13. Temp, Power

C : Commercial, Normal (0°C ~ 70°C)
L : Commercial, Low (0°C ~ 70°C)
I : Industrial, Normal (-40°C ~ 85°C)
P : Industrial, Low (-40°C ~ 85°C)

14~15. Speed (Wafer/Chip Biz/BGD: 00)

CC : DDR400 (200MHz @ CL=3, tRCD=3, tRP=3)
B3 : DDR333 (166MHz @ CL=2.5, tRCD=3, tRP=3)
AA : DDR266 (133MHz @ CL=2, tRCD=2, tRP=2)
A2 : DDR266 (133MHz @ CL=2, tRCD=3, tRP=3)
B0 : DDR266 (133MHz @ CL=2.5, tRCD=3, tRP=3)

DDR SDRAM Code Information(2/2)

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<u>K</u>	<u>4</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>-</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17 18

16. Packing "Packing Type Reference"

- Common to all products, except of Mask ROM
- Divided into TAPE & REEL(In Mask ROM, divided into TRAY, AMMO Packing Separately)

Divide	Packing Type	New Marking
Component	TAPE & REEL	T
	Other (Tray, Tube, Jar)	0 (Number)
	Stack	S
Module	MODULE TAPE & REEL	P
	MODULE Other Packing	M

17~18. Customer "Customer List Reference"