

SDRAM Module Code Information

Last Updated : August 2009

<u>M</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>-</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

1. Memory Module(M)

2. Module Configuration

3 : 4/8 Byte DIMM (100, 168, 200, 232, 278pin)
 4 : 8 Byte SODIMM (144pin)

3~4. Data bits

23 : x144/ECC PLL+Register DIMM
 63 : x64 micro DIMM with SPD
 64 : x64 PC100 SODIMM with SPD
 66 : x64 U-DIMM/SODIMM with SPD
 74 : x72/ECC U-DIMM with SPD
 78 : x72/ECC PLL+Register DIMM with SPD
 for 200pin (JEDEC)
 90 : x72/ECC PLL+Register DIMM with SPD
 for 168pin (RCC)

5. Feature, Voltage

S : SDRAM, 3.3V

6~7. Depth

04 : 4M	08 : 8M
09 : 8M (for 128Mb/512Mb)	16 : 16M
17 : 16M (for 128Mb/512Mb)	28 : 128M
29 : 128M (for 128Mb/512Mb)	32 : 32M
33 : 32M (for 128Mb/512Mb)	56 : 256M
64 : 64M	
65 : 64M (for 128Mb/512Mb)	

8. Refresh, # of banks, Interface

2 : 4K/64ms Ref., 4Bank, LVTTL
 5 : 8K/64ms Ref., 4Bank, LVTTL

9. Composition Component

0 : x4 3 : x8
 4 : x16
 8 : x4 Stack
 9 : x8 Stack

10. Component Generation

M : M-die	A : A-die
B : B-die	C : C-die
D : D-die	E : E-die
F : F-die	G : G-die
H : H-die	I : I-die
K : K-die	

11. Package

L : TSOP2 (Lead-Free, Halogen-Free)
 N : sTSOP2 K : TSOP2-400 (DDP)
 T : TSOP2-400
 U : TSOP2-400 (Lead-Free)
 V : sTSOP2 (Lead-Free)
 6 : sTSOP2 (Lead-Free, Halogen-Free)

12. PCB Revision & Type

0 : Mother PCB	1 : 1st Rev.
2 : 2nd Rev.	3 : 3rd Rev.
4 : 4th Rev.	
S : 4Layer PCB	

13. "—"

14. Power

C : Normal, Self Ref. L : Low, Self Ref.

15~16. Speed (tCC: Default CL3)

10 : 10ns PC66
 1H : 10ns @CL2 PC100
 1L : 10ns PC100
 75 : 7.5ns PC133
 7A : PC133 3-3-3 + PC100 2-2-2
 7C : 7.5ns PC133 2-2-2

17~18. Customer (Special Handling)

"Customer List Reference"