

# Sync DRAM Code Information(1/2)

Last Updated : May 2008

<b>K</b>	<b>4</b>	<b>X</b>	<b>X</b>	<b>X</b>	<b>X</b>	<b>X</b>	<b>X</b>	<b>X</b>	<b>X</b>	<b>-</b>	<b>X</b>	<b>X</b>	<b>X</b>	<b>X</b>	<b>X</b>	<b>X</b>	
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

## 1. Memory (K)

2. DRAM : 4

## 3. Small Classification

S : SDRAM

## 4~5. Density, Refresh

16 : 16M, 2K/32ms  
 28 : 128M, 4K/64ms  
 51 : 512M, 8K/64ms  
 56 : 256M, 8K/64ms  
 64 : 64M, 4K/64ms  
 1G : 1G, 8K/64ms

## 6~7. Organization

04 : x4  
 06 : x4 Stack  
 07 : x8 Stack  
 08 : x8  
 16 : x16  
 32 : x32

## 8. Bank

2 : 2 Bank  
 3 : 4 Bank

## 9. Interface, VDD, VDDQ

2 : LVTTTL, 3.3V, 3.3V  
 L : LVCMOS, 2.5V, 2.5V

## 10. Generation

11. “—”

## 12. Package

N : STSOP2  
 T : TSOP2  
 U : TSOP2 (Lead-Free)  
**L : TSOP2 (Lead-Free & Halogen-Free)**  
 V : STSOP2 (Lead-Free)

Note : In a special case, TSOP2 package code “-U” of SDR 256Mb J-die/128Mb K-die and sTSOP2 “V” of 256Mb J-die stand for Lead-free and Halogen free,

## 13. Temp, Power

C : Commercial, Normal ( 0°C ~ 70°C )  
 L : Commercial, Low ( 0°C ~ 70°C )  
 I : Industrial, Normal ( -40°C ~ 85°C )  
 P : Industrial, Low ( -40°C ~ 85°C )  
 E : Extended, Normal ( -25°C ~ 85°C )  
 N : Extended, Low ( -25°C ~ 85°C )

## 14~15. Speed ( Wafer / Chip Biz / BGD : 00 )

50 : 5ns  
 55 : 5.5ns  
 60 : 6ns  
 70 : 7ns  
 75 : 7.5ns, PC133  
 80 : 8ns

# Sync DRAM Code Information(2/2)

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<u>K</u>	<u>4</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>-</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

## 16. Packing “Packing Type Reference”

- Common to all products, except of Mask ROM
- Divided into TAPE & REEL(In Mask ROM, divided into TRAY, AMMO Packing Separately)

Divide	Packing Type	New Marking
Component	TAPE & REEL	T
	Other ( Tray, Tube, Jar )	0 ( Number)
	Stack	S
Module	MODULE TAPE & REEL	P
	MODULE Other Packing	M

## 17~18. Customer “Customer List Reference”