# Idd6 Low power mode for DDR Registered DIMM.

Written by Gye .Won. Ha. 11/30 ' 01

## Introduction.

There are two possible status of PLL and register(s) at self refresh mode depends on the state of the external clock. In order to achieve low self-refresh current from registered DIMM, external clock should be shut off. Otherwise, current consumption from DLL & register(s) a lot bigger than current from total DRAM on the registered DIMM.

DDR SDRAM has two differedt self-refresh mode;

1. PLL & regisrer(s) are enabled
2. PLL & regisrer(s) are disabled(power down)

This application note describes how to achieve low self-refresh current with DDR registered DIMM.

## Clock driver on &off current comparison.

Table 2 show self refresh current SPEC in registered DIMM for 512MB(M383L6420BT1)

Total Idd6 (for 512MB (x4) registered DMM ) = Idd6 x 18 + Iclock_on + Ireg_on
= 3mA x 18 + 300mA = 354mA. in case of normal power Idd6

Note : Iclock_on : Current from PLL(Clock toggles)
Iclock_off : Current from PLL(Clock disables)
Ireg_on : Current from Register(non-power down)
Ireg_off : Current from Register(power down)

| Symbol | | K4H560438B-TCA2 (DDR266A) | | K4H560438B-TCB0 (DDR266B) | | K4H560438B-TCA0 (DDR200) | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | typical | worst | typical | worst | typical | worst | | |
| IDD6 | Normal | 3 | 3 | 3 | 3 | 3 | 3 | mA | |
| | Low power | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | 1.5 | mA | Optional |

**Table 1 : self refresh current for 256Mb ( K4H560438B-T)**

| Symbol | | A2(DDR266@CL=2) | | B0(DDR266@CL=2.5) | | A0(DDR200@CL=2) | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | typical | worst | typical | worst | typical | worst | | |
| IDD6 | Normal | 354 | 354 | 354 | 354 | 354 | 354 | mA | |
| | Low power | 327 | 327 | 327 | 327 | 327 | 327 | mA | |

**Table 2 : self refresh current for 512MB ( M383L6420BT1)**

As Table 3 show, self refresh currents in registered DIMM practically have a different values according to PLL on/off. These currents were measured by tester with 4 vendor's. All DIMMs measured are 512MB and obtained in 100Mhz, Room temp. PLL on is that both PLL and register are turned on. PLL off means both PLL and register are turrned off. if frequency increase, each currents where PLLs are turned on goes up also.

Unit : mA

| | 512Mbyte | 512Mbye | 512Mbyte | 512Mbye |
|---|---|---|---|---|
| PLL Vendor | A | B | C | D |
| VDD = 2.7V PLL OFF | 35.2 | 33 | 33.4 | 34 |
| VDD = 2.7V PLL ON | 255.6 | 280 | 325.2 | 348.8 |
| VDD = 2.5V PLL OFF | 32.2 | 29.8 | 31.8 | 31 |
| VDD = 2.5V PLL ON | 232.4 | 254.8 | 295 | 319.2 |
| VDD = 2.3V PLL OFF | 31.6 | 29.4 | 29.6 | 30 |
| VDD = 2.3V PLL ON | 210 | 227.8 | 266.6 | 289.4 |

**Table 3 : self refresh currents in 512MB measured by tester ( M383L6420BT1)**

The PLL enters power down mode automatically when the external clock stops toggling or down to less than 20Mhz.

## The sequence of self refresh entry for power down mode of registered DIMM.

1. The system applies self refresh command.(CKE, CS, RAS, CAS are all low and WE is high state.)
   Note : The commands is delievered to the DDR SDRAM one clock later due to the additional register pipelining.
2. The system sets $\overline{\text{RESET}}$ at a vaild low level for register power down.
   This input condition forces all register output to a low state independent on the condition on the register inputs.
3. The system turns off clock inputs to the DIMM.
   This must be done after the $\overline{\text{RESET}}$ deactive time of the register (t(INACT)).
   The chipset must continue to hold valid data and clock signals on the register inputs until the differential receivers are powered down completely. This time is called t(INACT) , the time it takes for the differential receivers to become inac - tive after RESET goes low.

Figure 1 show the power down sequence of self refresh entry in registered DIMM.

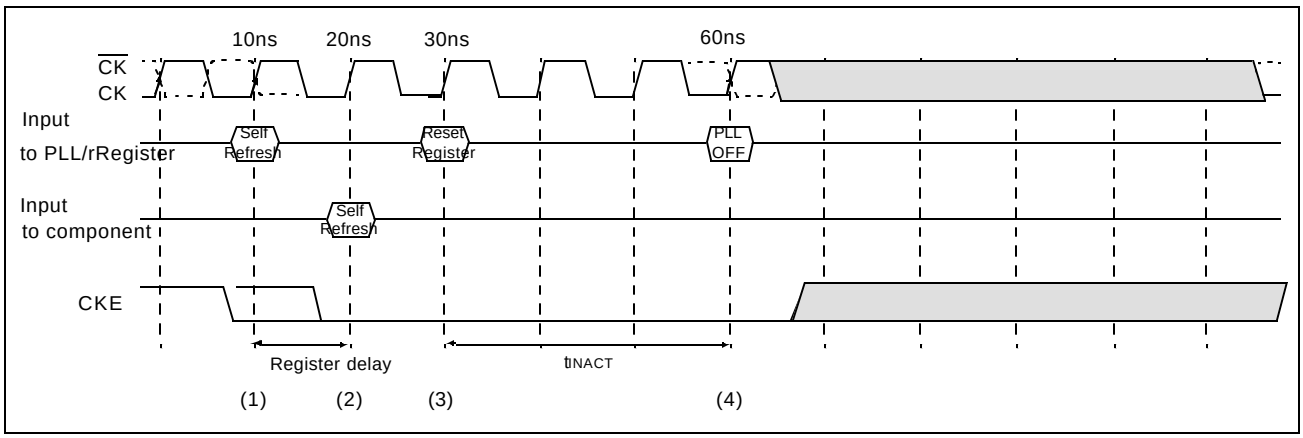


**Figure 1. Power down sequence for self refresh (DDR200)**

(1) Self refresh command input from the memory controller to register input pin on registered DIMM.
(2) Self refresh command input to component input pin after 1CLK delay from register.
(3) Reset input to register on registered DIMM.
(4) Turn off clock driver after t(INACT).

## The sequence of self refresh exit .

1. The system initially must supply a clock signal to clock driver on registered DIMM.
   The clock driver (PLL) requires specific time to stabilize after receiving a valid clock. After this time, the register sees a stable clock at its clock inputs. CKE must be maintained low and all other inputs should be driven to a known state.
2. The system applies valid logic level to the data input of the register during stabilization of the clock driver.
3. The system switches $\overline{\text{RESET}}$ to a logic high level for register on.
   That means SDRAM is now functional and prepared to receive commands.
4. The system must maintain stable register inputs until normal register operation is attained.
5. After the specified tACT has elapsed, the system issues the NOP command. This command is clocked through the now fully operational register to the SDRAM. The chipset then takes the CKE line high, and the SDRAM exits self-refresh mode. This is clocked through the register as well.
   tACT is the time from RESET high until the inputs are fully enabled. The chipset designers have to know how long the register takes to become stable.
6. Then, the chipset can begin the JEDEC-defined exit self-refresh procedure, after which the DDR SDRAM is ready for normal operation.

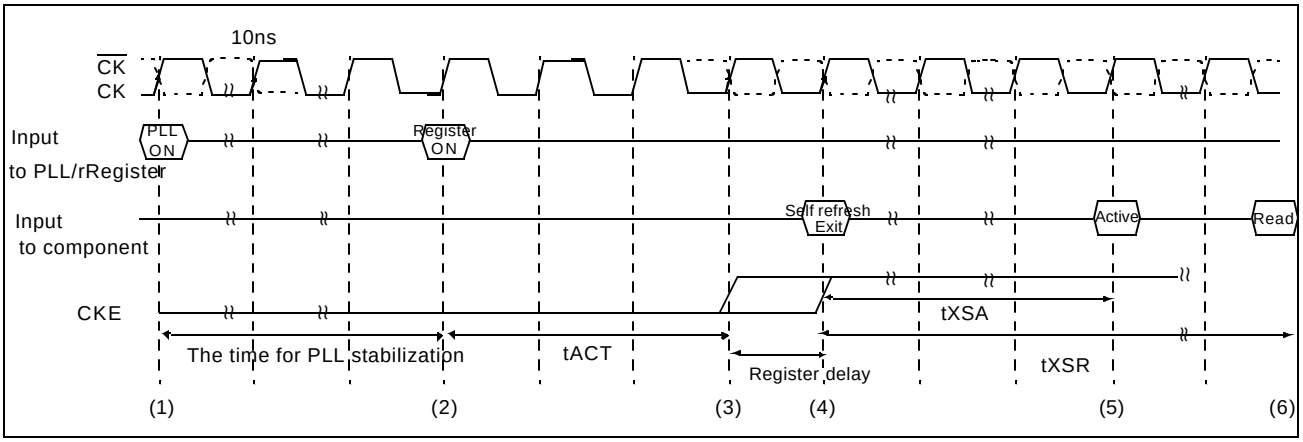


**Figure 1. The sequence for self refresh exit (DDR200)**

(1) Clock input from the memory controller to clock driver on registered DIMM.
(2) High level input to $\overline{\text{RESET}}$ pin of register after the time for stabliization of clock driver.
(3) CKE high input to register after tACT
(4) CKE high input to DDR SDRAM after 1CLK delay from register.
(5) Active command input to component pin after guranteeing tXSA.
tXSA i s exit self refresh to bank active command, a write command can be applied as far as tRCD is satisfied after any bank active command.
(6) Read/write input to DDR SDRAM after tXSR.
tXSR is exit self refresh to read command.