

Date : July , 2003 (Revision 0.0)

Application Note

GDDR2 ODT On/Off Control Method (Single Rank / Dual Rank)

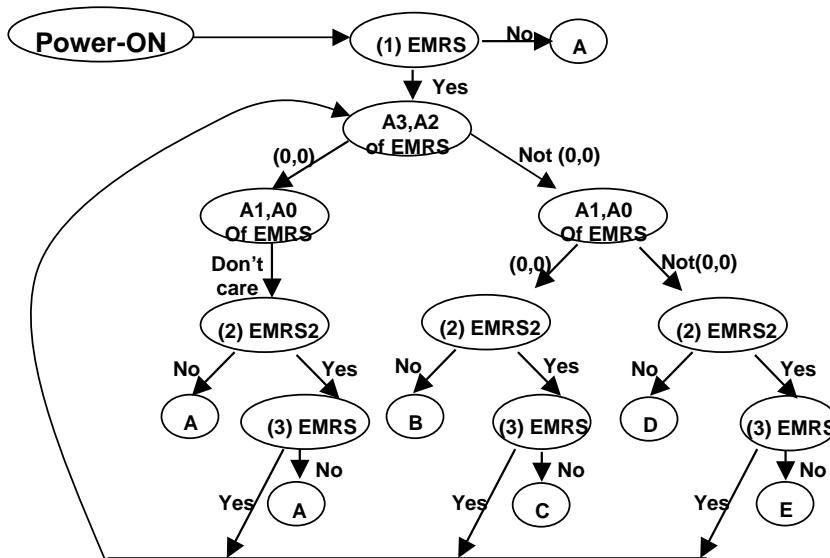
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How to enable the ODT

❖ Sequence of Issuing EMRS Command



❖ ODT control state diagram



<Table 1 > ODT status of each Pin

| Branch | CKE | CK, /CK | CS | CMD, Add | DQ,DM DQS, /DQS |
|--------|---------|---------|---------|----------|-----------------|
| A | Disable | Disable | Disable | Disable | Disable |
| B | Disable | Enable | Disable | Disable | Enable |
| C | Disable | V | Disable | Disable | Enable |
| D | Enable | Enable | Enable | Enable | Enable |
| E | V | V | V | Enable | Enable |

V : ODT status of each pin depends on EMRS2 code

ODT Control mode by EMRS&EMRS2

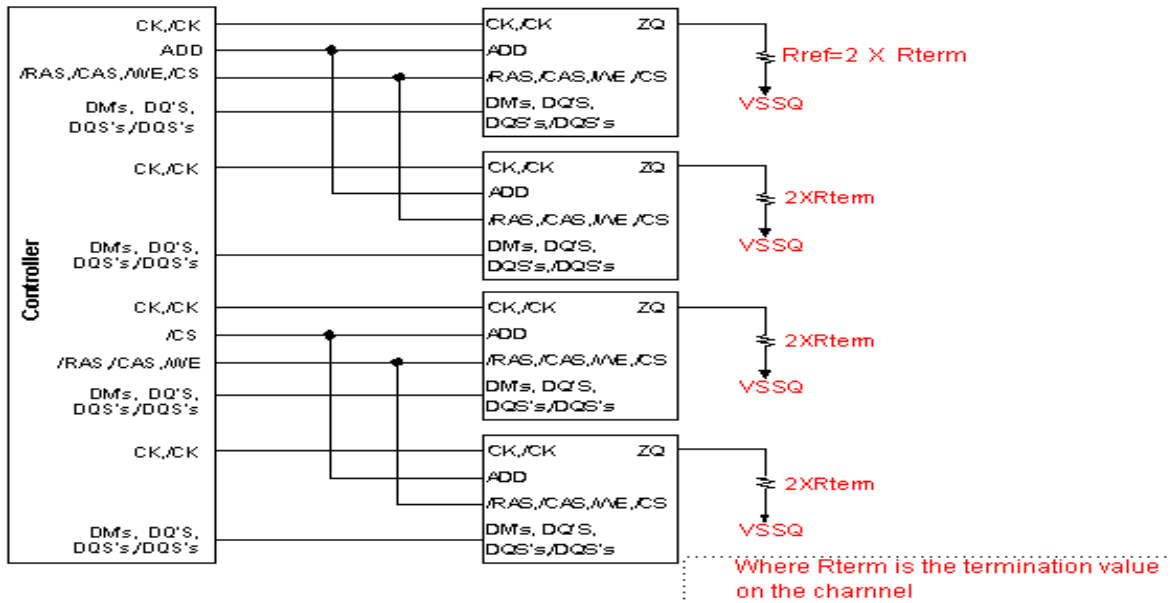
| MODE | EMRS CODE | | | | | EMRS2 CODE | | | | | | | ODT status of Pins | | | | |
|------|-----------|-------------|----|------------|----|------------|------------|-----------|----|-----------|----|-----------|--------------------|---------|-----|-----------------------|----------------|
| | Sys-tem | ODT control | | ODT option | | ODT W | ODT of CKE | ODT of CS | | ODT of CK | | ODT at Pd | CKE | CK, /CK | /CS | CMD Add Except /CSpin | DQ DM DQS /DQS |
| | A10 | A3 | A2 | A1 | A0 | A9 | A8 | A7 | A6 | A5 | A4 | A2 | | | | | |
| All | x | 0 | 0 | x | x | x | x | x | x | x | x | x | OFF | OFF | OFF | OFF | OFF |
| | x | Not (0 0) | | 0 | 0 | v | x | x | x | v | v | v | OFF | v | OFF | OFF | v |
| | x | Not (0 0) | | Not (0 0) | | v | 0 | 0 | 0 | 0 | 0 | v | OFF | OFF | OFF | v | v |
| | x | Not (0 0) | | Not (0 0) | | v | v | v | v | v | v | v | v | v | v | v | v |

<Table 2 > ODT status of each Pin by EMRS&EMRS2

- ODT can be controlled by EMRS & EMRS2 after power-up regardless of system configuration
- If no EMRS command issued, the ODT is controlled same as on page 12 in the spec.
- If EMRS2 command issued, the ODT value of each pin can be decided by A9~A2 value.
- ODTW Mode control scheme
 If A9 = 1 & WL=1 , the ODT for DQ,DQS,/DQS,DM are always enabled and those can be disabled only in case of Self-Refresh & Power Down mode
 If A9 = 0, & WL ≠ 1, the ODT can be enabled only after write command issued.
Thus, to save system power, it is recommended to set A9=0 & WL >4
- ODT at PD mode control
 If A2 =0, then the ODT for all pins except CK, /CK, CKE become disabled and accordingly no command can be issued.
 If A2=1 & dual rank, then cmd pins' ODT become enabled, thus a valid cmd can be issued
However, single rank system case, ODT at Pd mode should be always off.
 For the power saving purpose of dual rank system, if power down mode frequently used for one external rank DRAM while the other rank DRAM is working, ODT at Pd mode is recommended.

ODT control of Single Rank System

❖ Block Diagram of Single Rank System



It is recommended that every channel has equivalent termination value.
The equivalent termination value of each pin can be controlled by EMRS and EMRS2 command.

Example) CK, /CK, DQ's, DM's, DQS's, /DQS's : Single load
Address pins, /RAS, /CAS, /WE, /CS, and CKE : Dual Load
-> To make equivalent termination value on every channel, A1,A0 of EMRS should be (1,0)

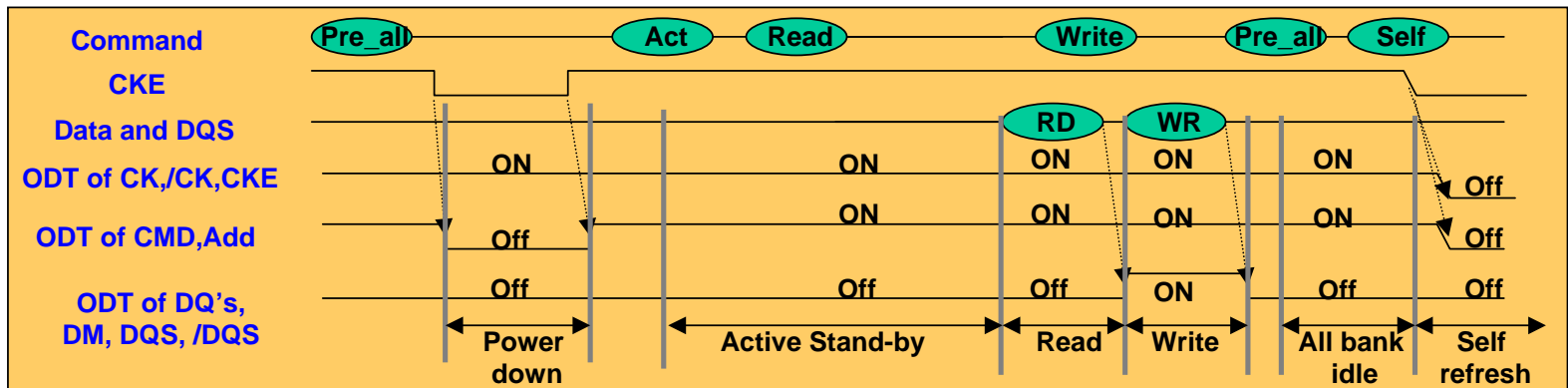
ODT On/Off Control of Single Rank System

| Mode | EMRS | EMRS2 Code | | MRS | ODT status of Pins | | |
|-----------------------------|--------|------------|-----------|------|--------------------|-------------|-------------------|
| | System | ODTW | ODT at Pd | WL | CK, /CK and CKE | CMD and Add | DQ, DM, DQS, /DQS |
| | A10 | A9 | A2 | | | | |
| Self Refresh / Fast wake-up | 0 | X | X | X | OFF | OFF | OFF |
| Power Down | 0 | X | X | X | ON | OFF | OFF |
| All bank idle | 0 | X | X | X | ON | ON | OFF |
| Active standby | 0 | 1 | X | X | ON | ON | ON |
| | | 0 | X | WL=1 | ON | ON | ON |
| Write | 0 | X | X | X | ON | ON | ON |
| Read | 0 | X | X | X | ON | ON | ON |

If A10 of EMRS is low, DRAM believes that the system has single rank. Thus, DWT, DRD and ODT control options at Power-down don't work to protect redundant ODT control operations.

When ODTW=1 or WL=1 is selected, ODT of DQ pins turn on to ready DQ channel for receiving Write Data always except self refresh and power-down mode.

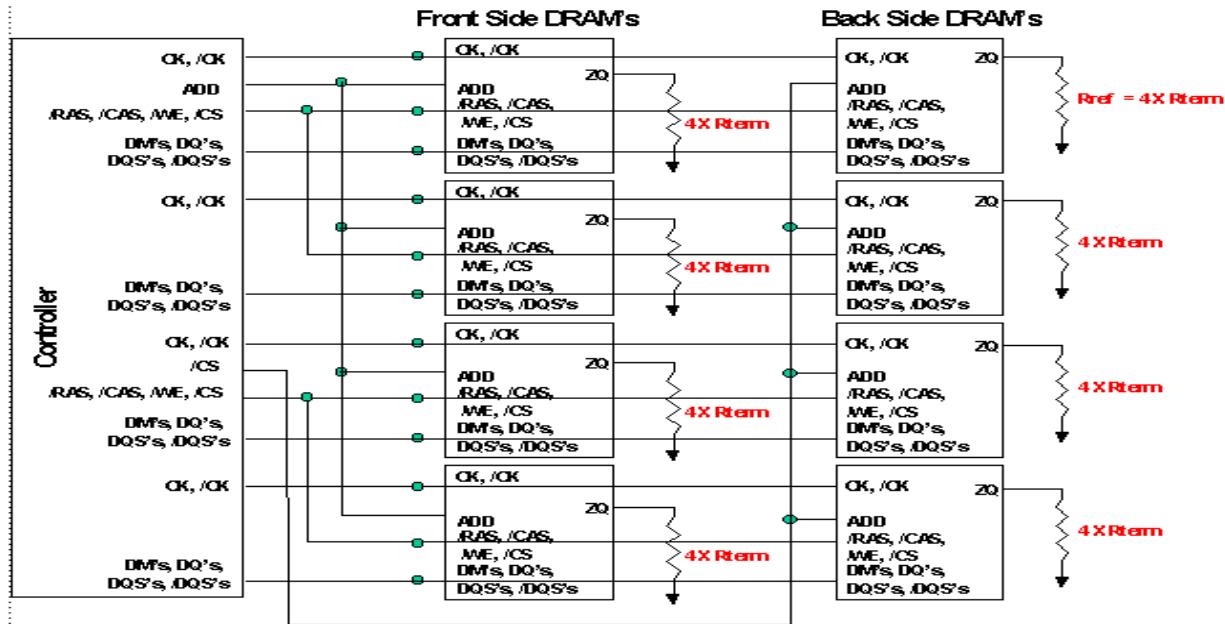
But when ODTW = 0 & WL≠1, ODT control timing diagram will be same as the followings.



< ODTW is enabled and WL≠1, ODT control timing >

ODT Control of Dual Rank System(I)

❖ Block Diagram of Dual Rank System



It is recommended that every channel has equivalent termination value.
The equivalent termination value of each pin can be controlled by EMRS and EMRS2 command.

For Example) CK, /CK, DQ's, DM's, DQS's, /DQS's : DUAL load
Address pins, /RAS, /CAS, /WE, /CS, and CKE : 4 DEVICES Load
=> To make equivalent termination value on every channel, A1,A0 of EMRS should be (1,0) and external resistor value of ZQ should be 2 times of single rank system's

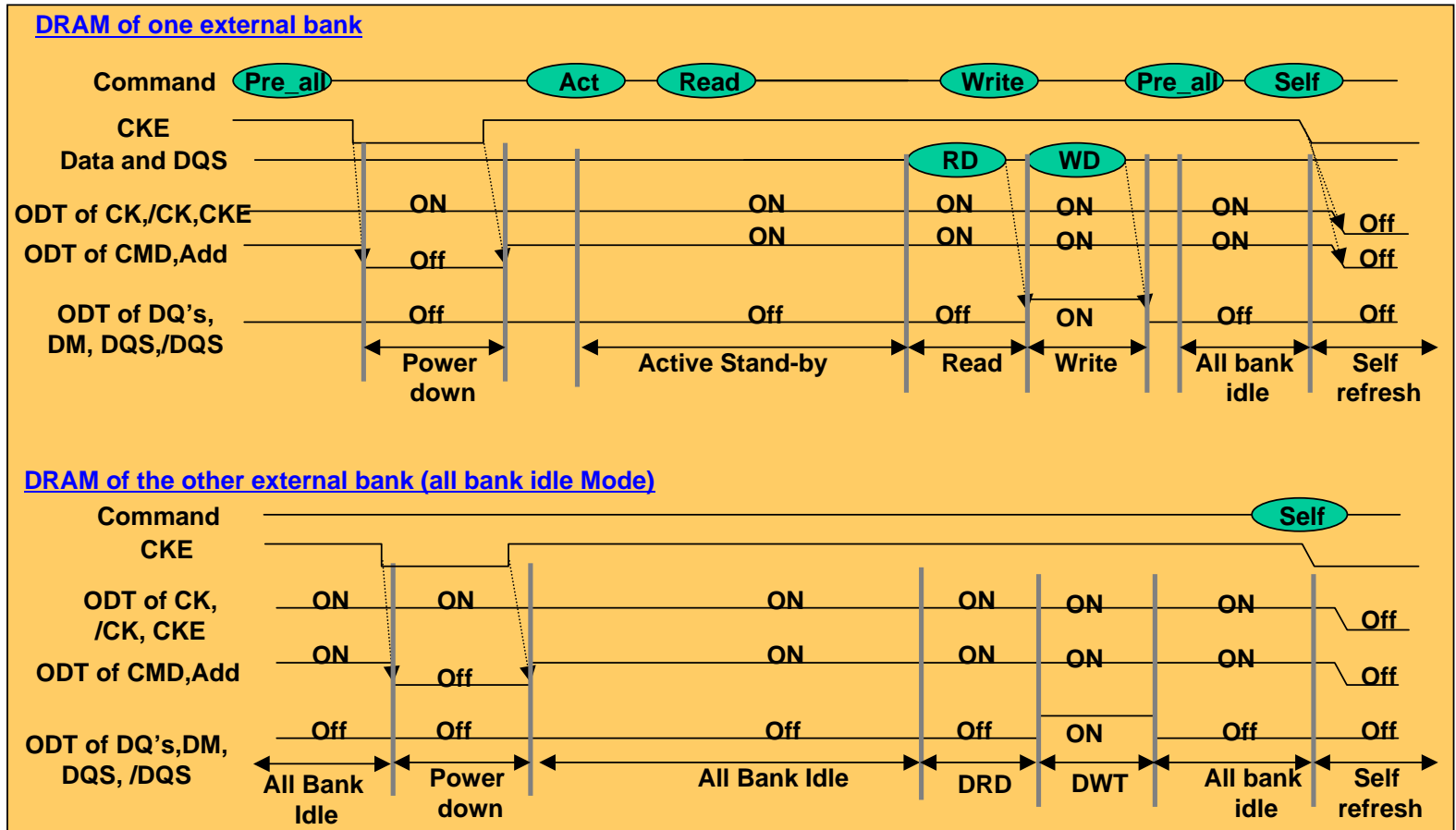
ODT Control of Dual Rank System(II)

| Mode | | EMRS | EMRS2 Code | | MRS | ODT status of Pins | | | ODT status of Pins | | | Remarks |
|--|--|--------|------------|-----------|------|---------------------------|-------------------|-------------------------|---------------------------|-------------------|-------------------------|----------------|
| DRAM1 | DRAM2 | System | ODTW | ODT at Pd | WL | CK, / CK and CKE | CMD and Add | DQ DM DQS .DQS | CK, / CK and CKE | CMD and Add | DQ DM DQS .DQS | |
| | | A10 | A9 | A2 | | | | | | | | |
| Self Refresh or Fast wake- up | Self Refresh or Fast wake- up | 1 | X | X | X | OFF | OFF | OFF | OFF | OFF | OFF | |
| | Other states | 1 | X | X | X | | | | | | | Illegal*1 |
| | Power Down | 1 | X | 0 | X | ON | OFF | OFF | ON | OFF | OFF | |
| Power Down | Other states | 1 | X | 0 | X | | | | | | | Illegal*1 |
| | | 1 | 1 | 1 | X | ON | ON | ON | ON | ON | ON | |
| | Power Down | 1 | 0 | 1 | WL=1 | ON | ON | ON | ON | ON | ON | |
| | | 1 | 1 | 1 | WL=1 | ON | ON | OFF | ON | ON | OFF | |
| | | 1 | 1 | 1 | X | ON | ON | ON | ON | ON | ON | |
| | Other states | 1 | 0 | 1 | WL=1 | ON | ON | ON | ON | ON | ON | DRD, DWT:Valid |
| All bank idle | | 1 | 1 | X | X | ON | ON | ON | ON | ON | ON | |
| | All bank idle | 1 | 0 | X | WL=1 | ON | ON | ON | ON | ON | ON | |
| | | 1 | 0 | X | WL=1 | ON | ON | OFF | ON | ON | OFF | |
| | | 1 | 1 | X | X | ON | ON | ON | ON | ON | ON | |
| All bank idle | Active standby | 1 | 0 | X | WL=1 | ON | ON | ON | ON | ON | ON | |
| | | 1 | 0 | X | WL=1 | ON | ON | OFF | ON | ON | OFF | |
| | Write | 1 | X | X | X | ON | ON | ON | ON | ON | ON | DWT of DRAM1 |
| | Read | 1 | X | X | X | ON | ON | OFF | ON | ON | OFF | DRD of DRAM1 |
| Active standby | | 1 | 1 | X | X | ON | ON | ON | ON | ON | ON | |
| | Active standby | 1 | 0 | X | WL=1 | ON | ON | ON | ON | ON | ON | |
| | | 1 | 0 | X | WL=1 | ON | ON | OFF | ON | ON | OFF | |
| | Write | 1 | X | X | X | ON | ON | ON | ON | ON | ON | DWT of DRAM1 |
| | Read | 1 | X | X | X | ON | ON | OFF | ON | ON | OFF | DRD of DRAM1 |

1. With these case, the system couldn't have suitable Rterm.
Because the on-die termination value on channel is two times than the target value.

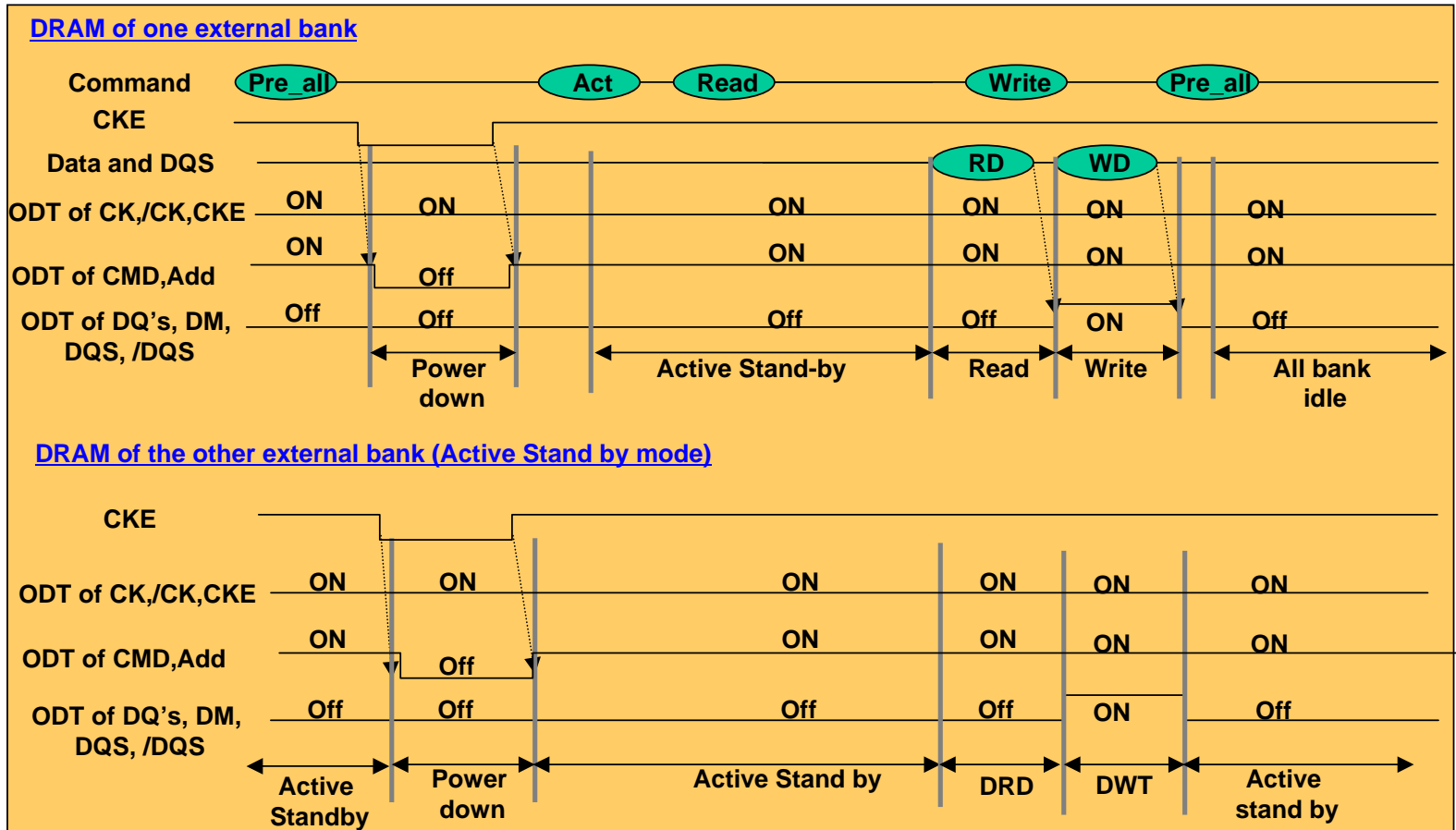
ODT On/Off Control of Dual Rank System(I)

1. **ODTW=0&WL≠1** and **ODT at Pd is off** while all bank Idle of the other external rank DRAM



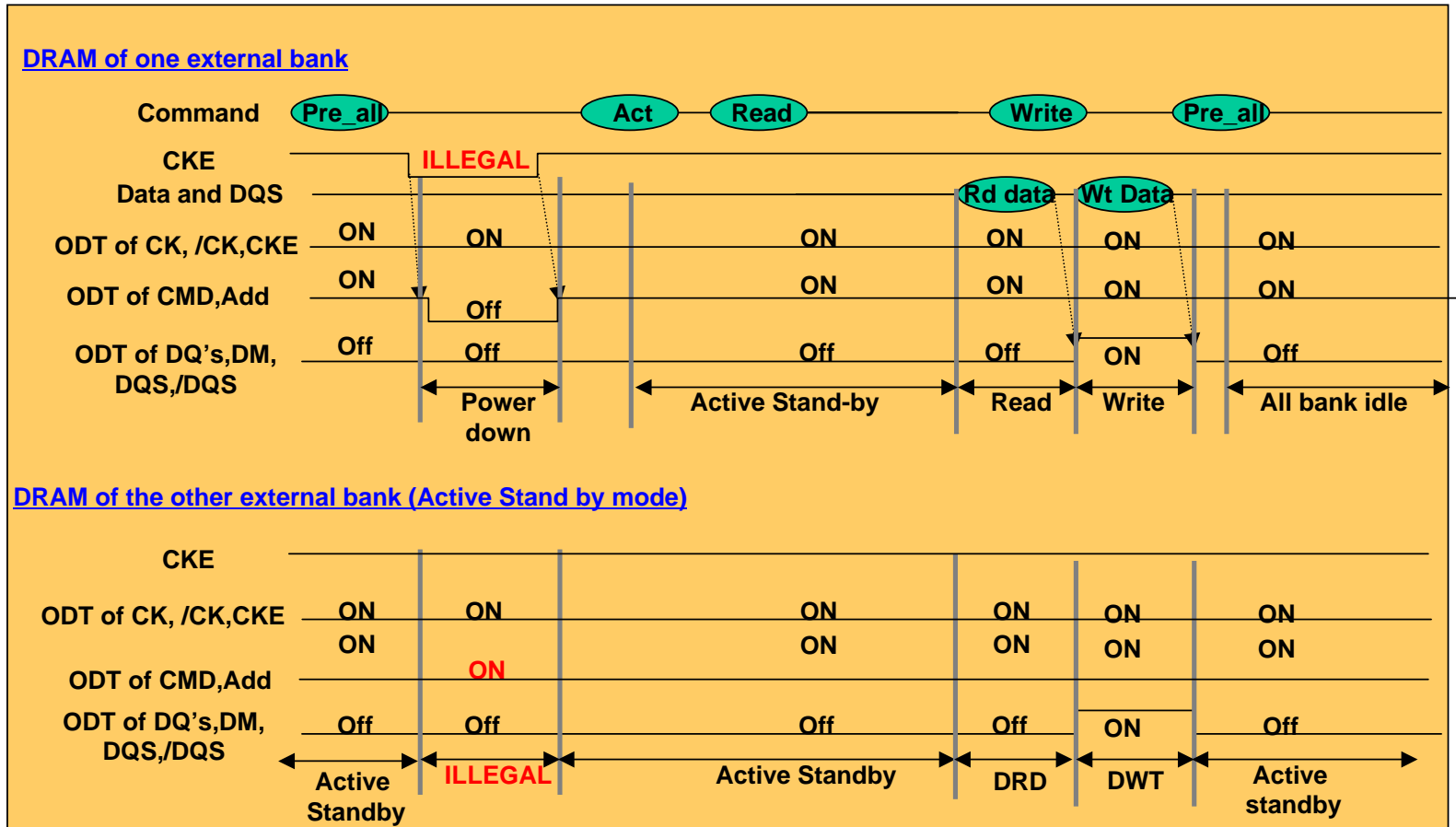
ODT On/Off Control of Dual Rank System(II)

2. ODTW=0&WL≠1 and ODT at Pd is off while Active Stand-by of the other external rank DRAM



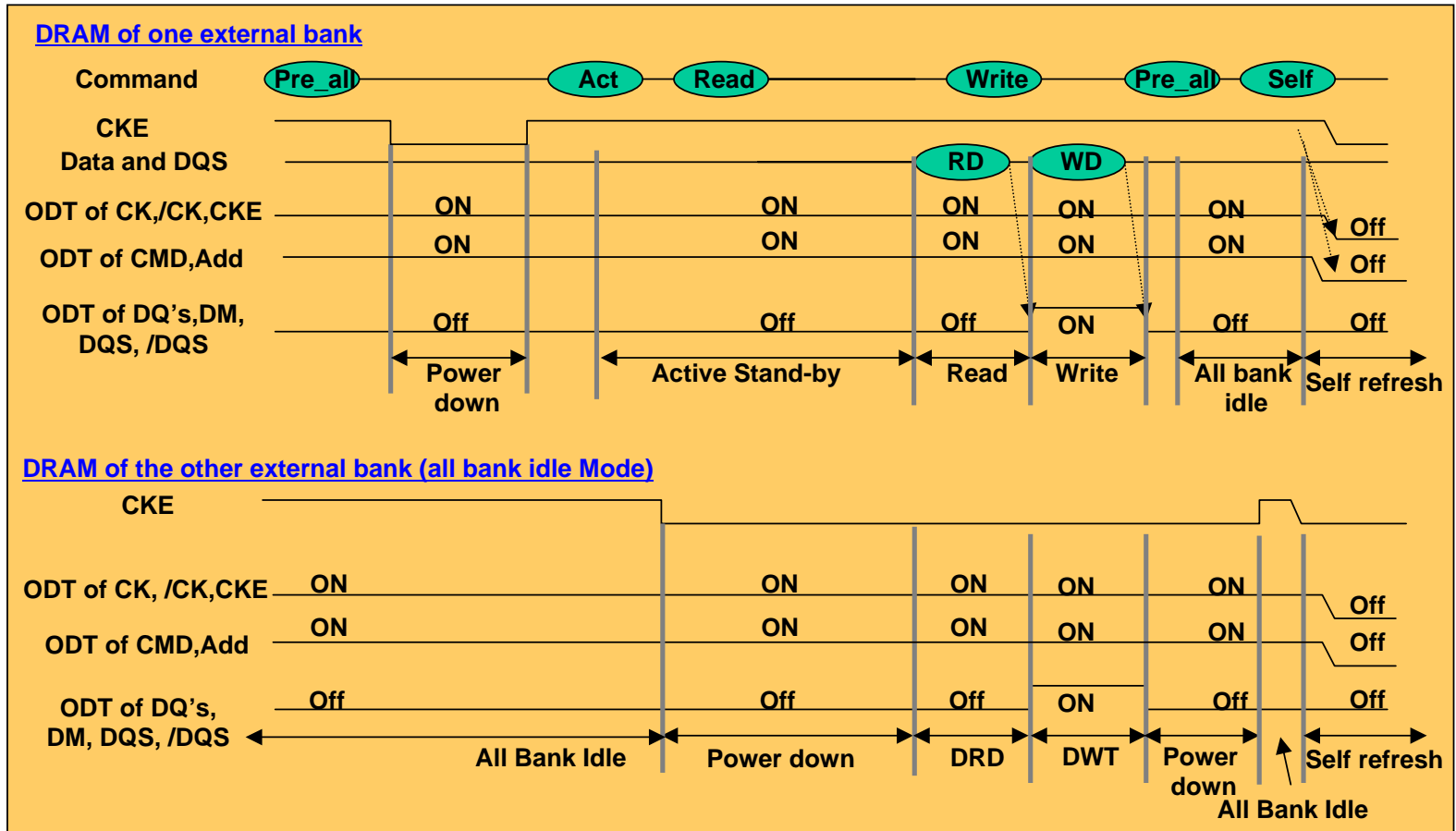
ODT On/Off Control of Dual Rank System(III)

3. ODTW=0 & WL≠1 and ODT at Pd is Off while Active Stand-by of the other external rank DRAM



ODT On/Off Control of Dual Rank System(IV)

4. ODTW=0& WL≠1 and ODT at Pd is On while All bank Idle of the other external rank DRAM



ODT On/Off Control of Dual Rank System(V)

5. ODTW=0& WL≠1 and ODT at Pd is On while Active Stand-by of the other external rank DRAM

