

*Application Note about*  
Registered DIMM spec. current calculation

Jan. '2002  
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# IDD calculation method @ 2 Row DIMM

Basically, Samsung DDR registered DIMM IDD spec is defined as below;

**Case 1** : { ( IDDx \* # of comp. Of row 1) + (IDD3N \* # of comp. Of row 2) +  
IDD(PLL + Register)} + 10% margin

**Case 2** : { ( IDDx \* # of comp. of row 1 & 2) + IDD(PLL + Register)} + 10% margin

## •Samsung DDR DIMM IDD spec table

Case	1 row condition	2 row condition
1	IDD0	IDD3N
1	IDD1	IDD3N
2	IDD2P	IDD2P
2	IDD2F	IDD2F
2	IDD2Q	IDD2Q
2	IDD3P	IDD3P
1	IDD3N	IDD3N
1	IDD4R	IDD3N
1	IDD4W	IDD3N
1	IDD5	IDD3N
2	IDD6	IDD6
1	IDD7	IDD3N

For example,

- # of chips : 36(stack)
- 1 row condition : IDD7  
(2 row condition : IDD3N)
- PLL current : 400mA
- Register current : 600mA
- Measured comp. IDD at IDD7 : 300mA
- Measured comp. IDD at IDD3N : 50mA
- Margin : 10%

**Total DIMM current =**

$$\{ (300*18) + (50*18) + 400 + 600 \} * 1.1$$

$$= \underline{8030 \text{ mA}}$$

# IDD calculation method @ 1 Row DIMM

Basically, Samsung DDR registered DIMM IDD spec is defined as below;

$$\{( \text{IDDx} * \# \text{ of comp. Of row 1} ) + \text{IDD(PLL + Register)}\} + 10\% \text{ margin}$$

For example,

- # of chips : 18
- IDD condition : IDD7
- PLL current : 400mA
- Register current : 600mA
- Measured comp. IDD at IDD7 : 300mA
- Margin : 10%

$$\text{Total DIMM current} = \{(300*18) + 400 + 600\} * 1.1 = \underline{7040 \text{ mA}}$$

# Register and PLL current @ 1GB DIMM

- PLL measured current (1 pcs on RDIMM)

PLL current (mA)	Power Down	133Mhz		100Mhz	
		max	min	max	min
2.3V	55.2	333.2	317.0	292.2	275.0
<b>2.5V *1</b>	57.2	<b>372.4</b>	352.2	326.8	306.0
2.7V	59.4	411.6	387.6	360.8	335.0

Note 1 : In calculating DIMM current, PLL current is considered as 400mA which is based on the current value @ 2.5V.

- Register measured current (2pcs on RDIMM)

Reg. current (mA)	at Toggle		at No_Toggle		Gap(Toggle - No_Toggle)	
	100Mhz	133Mhz	100Mhz	133Mhz	100Mhz	133Mhz
2.3V	339.4	480.8	28.2	31.4	314.2	449.4
<b>2.5V *1</b>	365.6	<b>537.6</b>	31.0	36.8	335.2	500.8
2.7V	394.4	591.8	37.0	42.8	357.6	550.4

Note 1 : In calculating DIMM current, Register current is considered as 600mA which is based on the current value @ 2.5V.

- **IDD(PLL) & IDD(Register) on spec: 400mA & 600mA**

# Samsung Stacked 1GB DIMM IDD spec

\*256Mb C-die component based

1 Row condition	2 Row condition	@ DDR200	@ DDR266
IDD0	IDD3N	3260	3560
IDD1	IDD3N	3660	4170
IDD2P	IDD2P	1180	1180
IDD2F	IDD2F	1900	1980
IDD2Q	IDD2Q	1660	1700
IDD3P	IDD3P	2050	2210
IDD3N	IDD3N	2065	2850
IDD4R	IDD3N	3700	4170
IDD4W	IDD3N	3820	4450
IDD5	IDD3N	4610	5010
IDD6	IDD6	1870	2010
IDD7	IDD3N	5920	6750

IDD(PLL) = 400mA, IDD(Reg.) = 600mA

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