

256Mb SDRAM Refresh cycle issue

- The difference compared to 128Mb SDRAM
 - Row address of CBR cycle : A0 - A11 --> A0 - **A12**
 - One CBR Interval : 4K/64ms (15.6us) --> **8K/64ms(7.8us)**
- To use 256Mb SDRAM,
the chipset and ROM BIOS should support the refresh cycle interval of 7.8us.
- If the chipset automatically changes the register value with SPD data,
there will not be any problem because the SPD data was registered with 7.8us.

ITEM	64Mb	Increase CA →	128Mb	Increase RA →	256Mb
Refresh	4K/64ms				8K/64ms
No. of Banks	4Banks				
x4	BS : BA0 - BA1 RA : A0 - A11 CA : A0 - A9		BS : BA0 - BA1 RA : A0 - A11 CA : A0 - A9, A11		BS : BA0 - BA1 RA : A0 - A12 CA : A0 - A9, A11
x8	BS : BA0 - BA1 RA : A0 - A11 CA : A0 - A8		BS : BA0 - BA1 RA : A0 - A11 CA : A0 - A9		BS : BA0 - BA1 RA : A0 - A12 CA : A0 - A9
x16	BS : BA0 - BA1 RA : A0 - A11 CA : A0 - A7		BS : BA0 - BA1 RA : A0 - A11 CA : A0 - A8		BS : BA0 - BA1 RA : A0 - A12 CA : A0 - A8