

Technical Note on tBC

This Application Note is applied to below products.

- K1B5616B2M, K1B5616BAM, K1B5616BBM, K1S5616BCM, K1S56161CM
- K1B2816B2A, K1B2816BAA, K1B2816BBA, K1S2816BCA, K1S28161CA

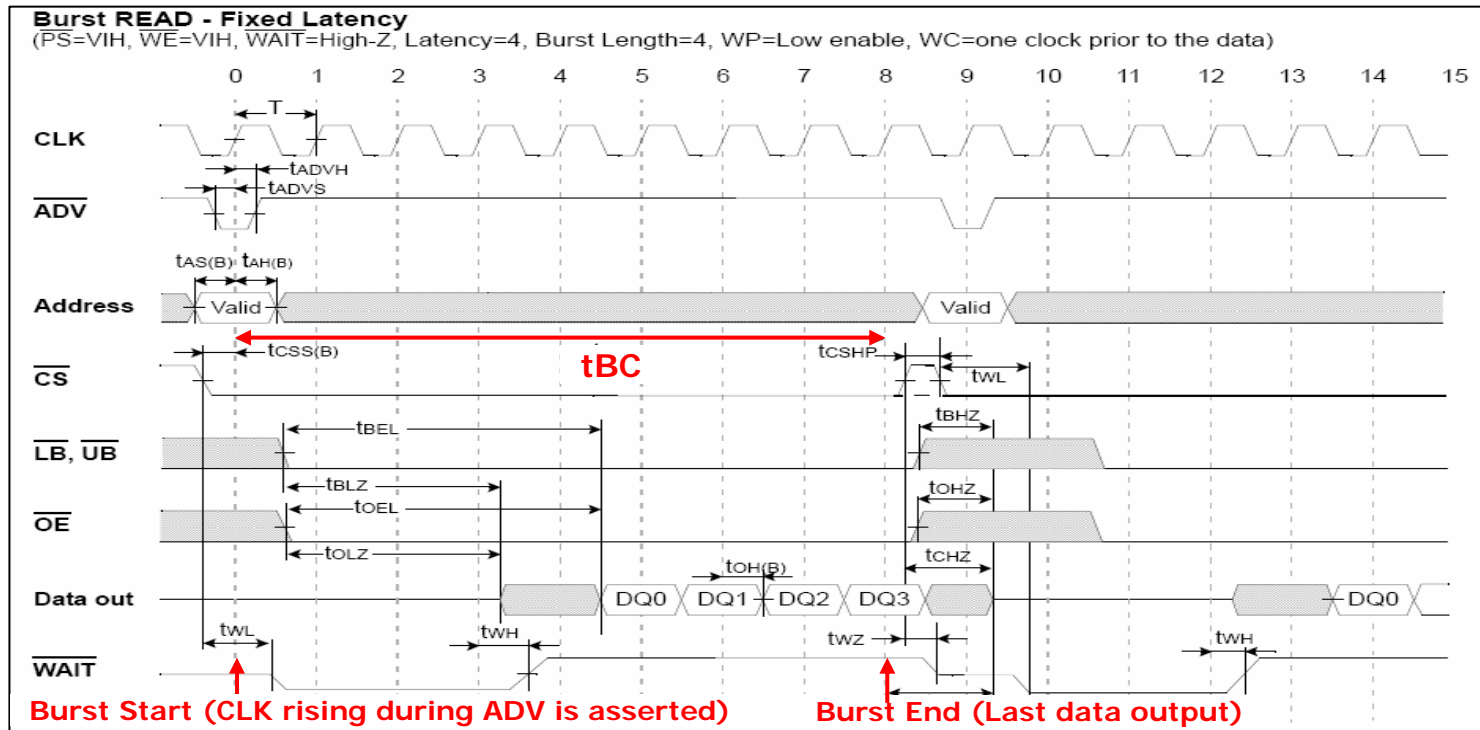
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Product Planning & Application Engineering Team

**MEMORY DIVISION
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Definition of tBC

AC CHARACTERISTICS									
Parameter List	Symbol	66MHz		80MHz		104MHz		Units	
		Min	Max	Min	Max	Min	Max		
Clock Cycle Time	T	15	200	12.5	200	9.6	200	ns	
Burst Cycle Time	tBC	-	1700	-	1700	-	1700	ns	
Address Set up Time to clock	tAS(B)	3		3		3		ns	



- * tBC is the time from the **Burst Read (Write) Start** to the **Burst Read (Write)End**.
 - * Refresh is denied during all the tBC.
 - * Refresh should be implemented in every 1.7us or the device stops all the function.
 (All Inputs: don't care. All outputs: low)
- tBC should not be longer than 1.7us

tBC & Burst Length

Frequency / Cycle time	Latency	Burst Length	tBC Cycle time * (Latency + Burst Length)
66Mhz / 15.0ns	3	32	0.53us
52Mhz / 19.2ns	3	32	0.67us
40Mhz / 25.0ns	2	32	0.85us
33Mhz / 30.0ns	2	32	1.02us
20Mhz / 50.0ns	2	32	1.70us
13Mhz / 76.9ns	2	32	2.64us (SPEC violation)
		16	1.38us
11Mhz / 90.9ns	2	16	1.64us
10Mhz / 100ns	2	16	1.80us (SPEC violation)

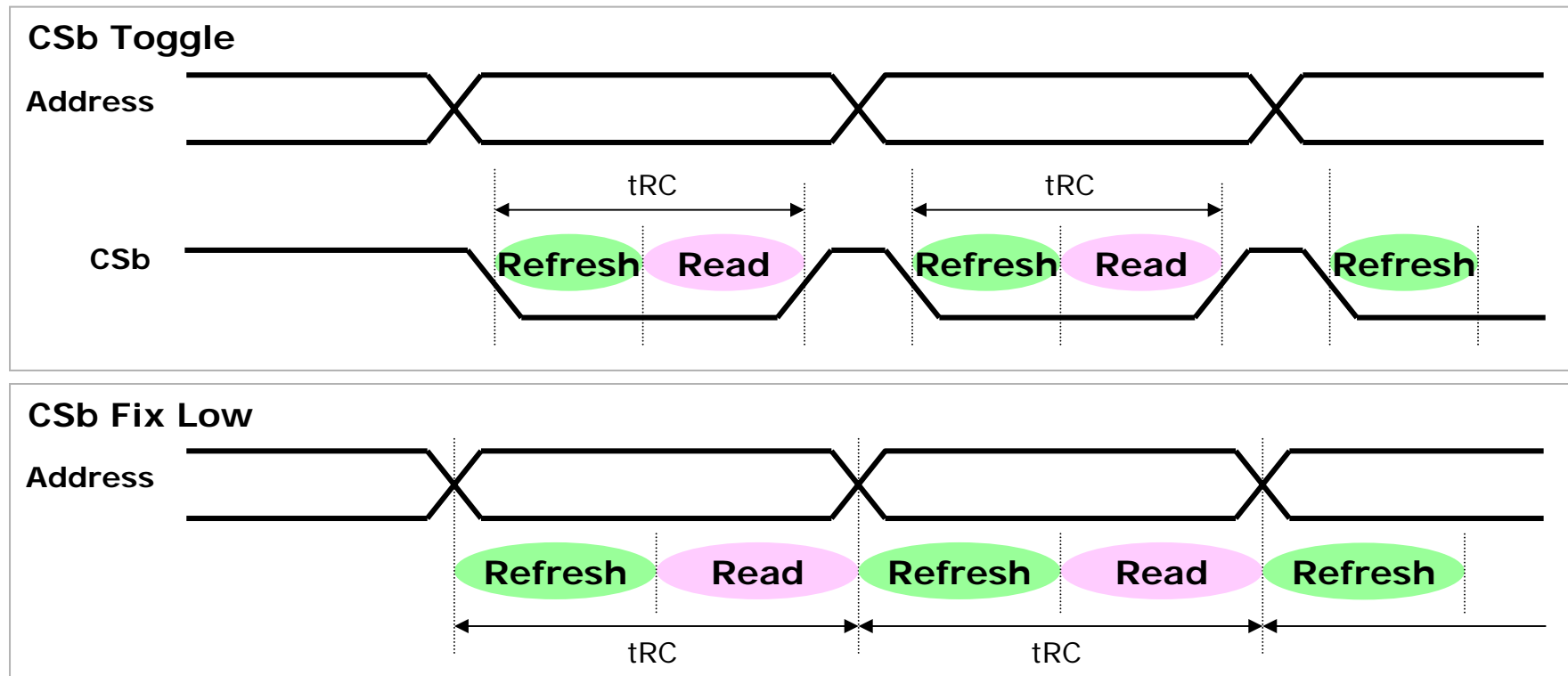
* The min. Frequency where 32 burst is available is **20Mhz**

* The min. Frequency where 16 burst is available is **11Mhz**

Refresh in Asynchronous operation

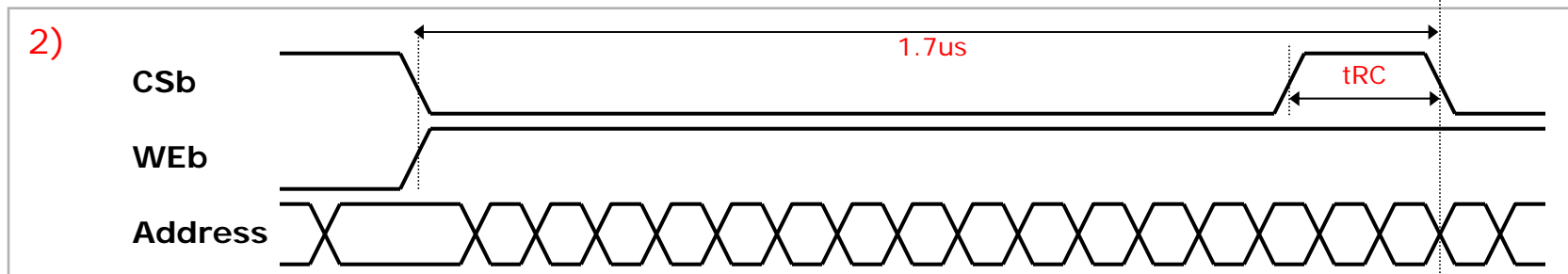
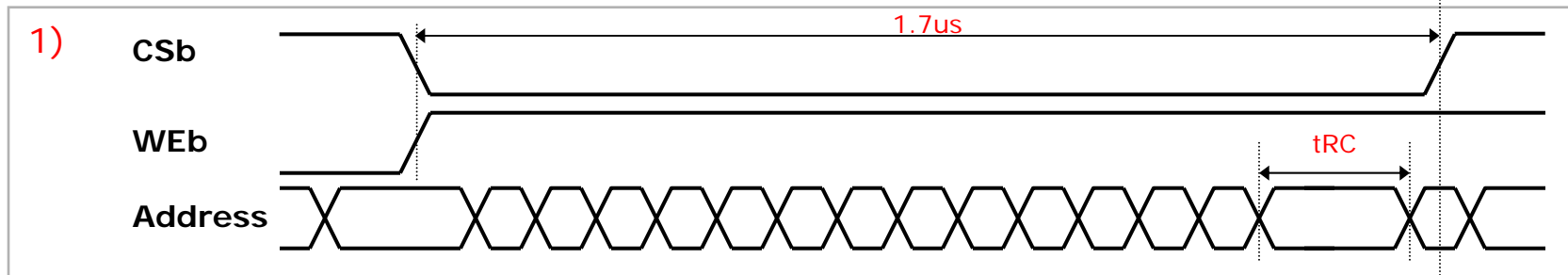
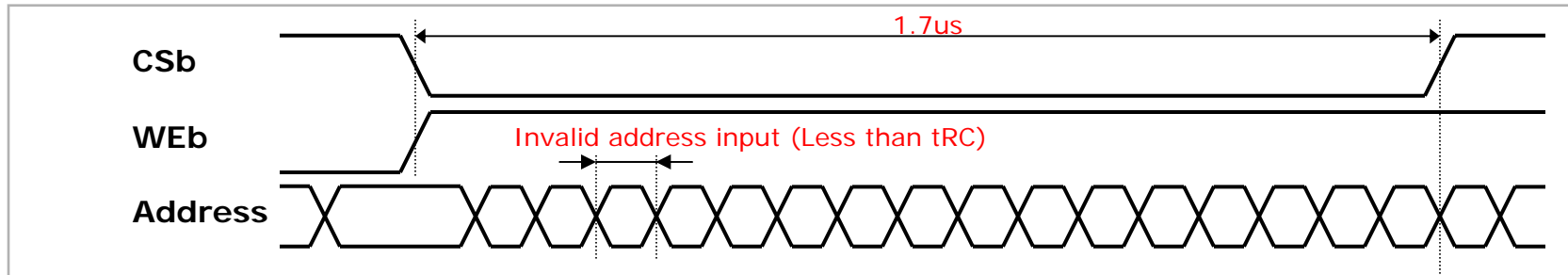
Asynch. READ

(PSb=VIH, WEb=VIH, WAIT=High-Z, UBb/LBb=LOW, OEb=LOW)



- * Each Read cycle (or Write cycle) contains refresh cycle in Asynchronous operation.
- * 1st half of Read cycle (or Write cycle) is dedicated to refresh cycle.
- * 2nd half of Read cycle (or Write cycle) is dedicated to actual Read cycle.
- There is no Refresh issue in normal Asynch Read (or Write) operation.

Refresh in Asynchronous operation



- * Refresh can not be properly implemented if invalid address input shorter than min. tRC is entered.
- * Invalid address input should not be repeated in a row for over 1.7us.
- The device needs a normal read timing(tRC¹⁾ or CS high for min. tRC²⁾ at least once in every 1.7us.