

Write method & Mode Change

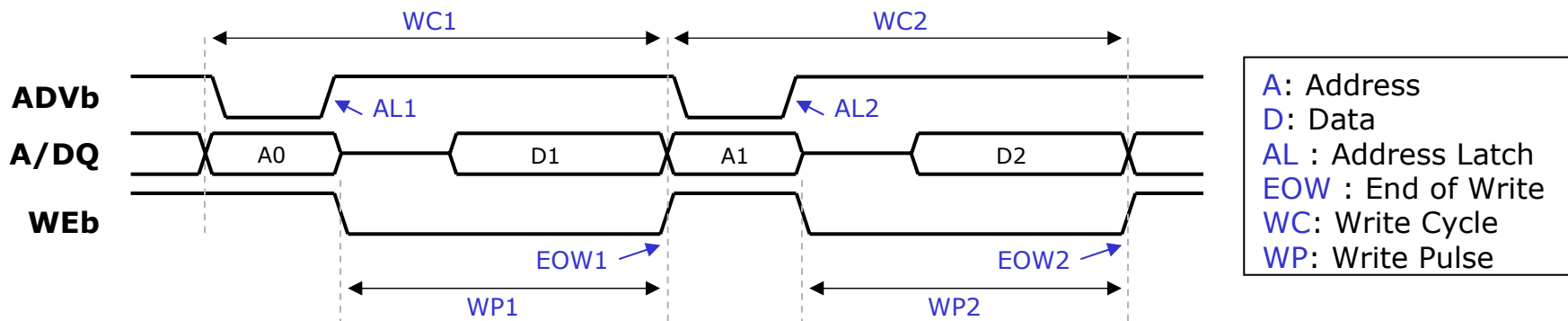
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Product Planning & Application Engineering Team

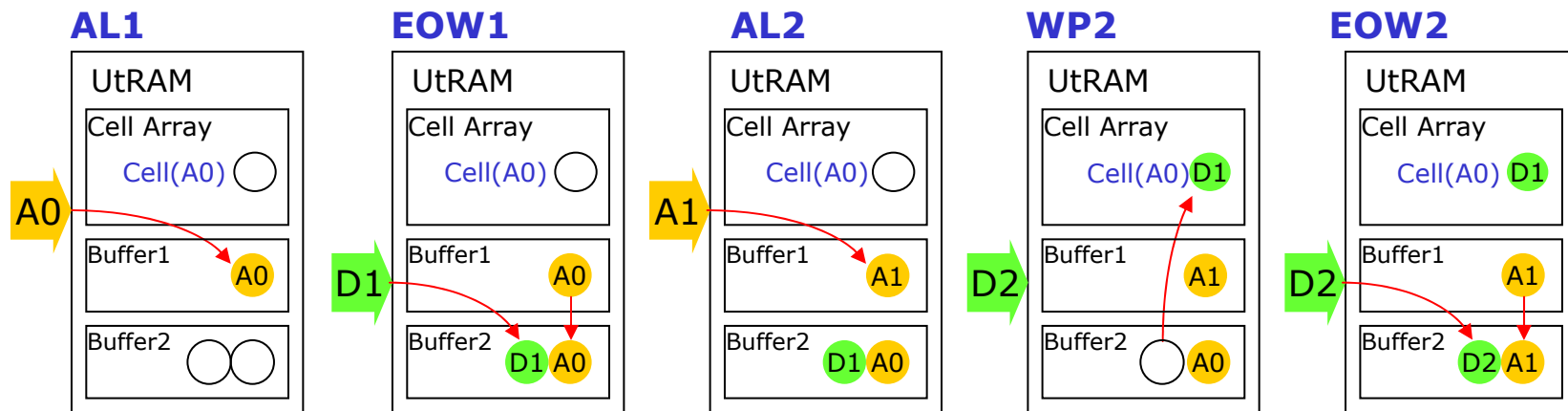
**MEMORY DIVISION
SAMSUNG ELECTRONICS Co., LTD**

UtRAM Write

Asynchronous Write



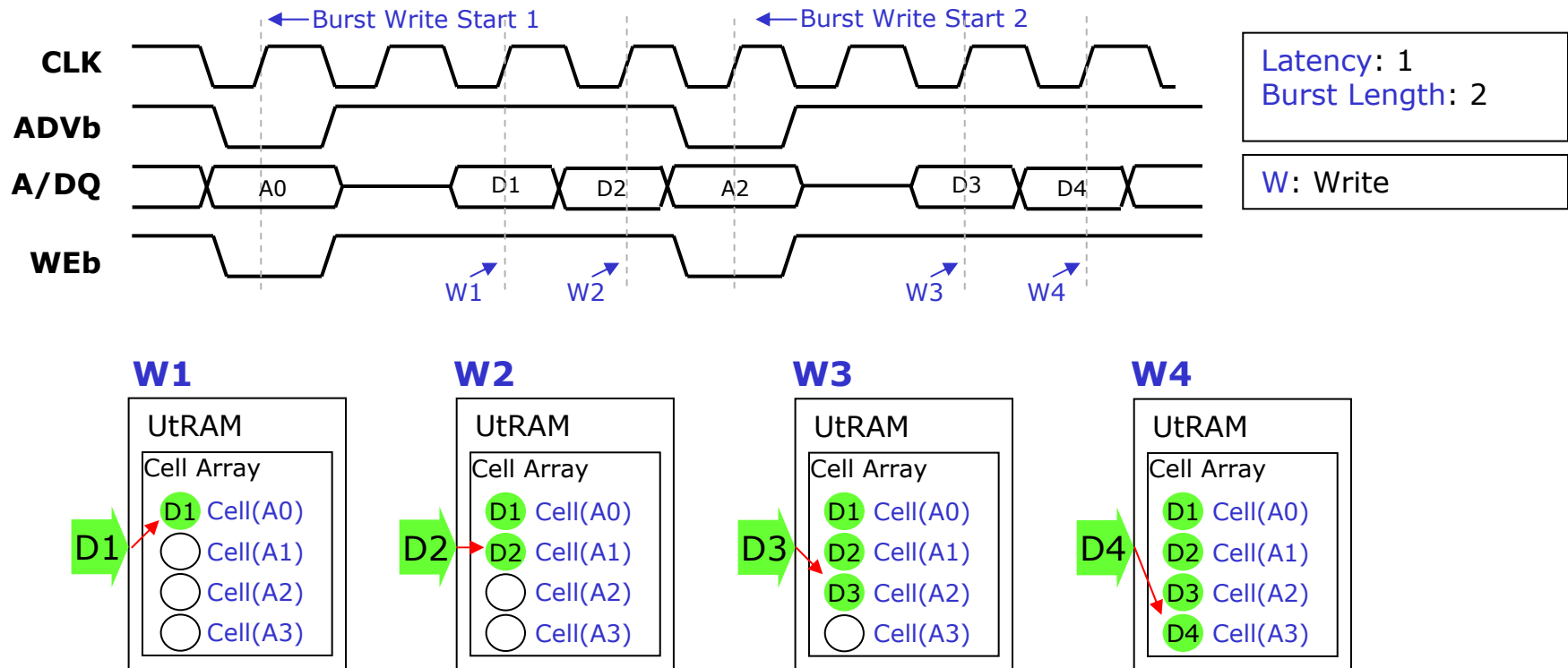
A: Address
 D: Data
 AL : Address Latch
 EOW : End of Write
 WC: Write Cycle
 WP: Write Pulse



- * UtRAM stores the current data in the buffer2 at the end of current write cycle and writes it to the cell during the next Write cycle. → **"Late Write"**
- * UtRAM accesses 'Buffer2' instead of 'Cell(A0)' when A0 is input for Read before WC2.
- * 'Late Write' is applied only for the **Asynchronous Write**.

UtRAM Write

Synchronous Write

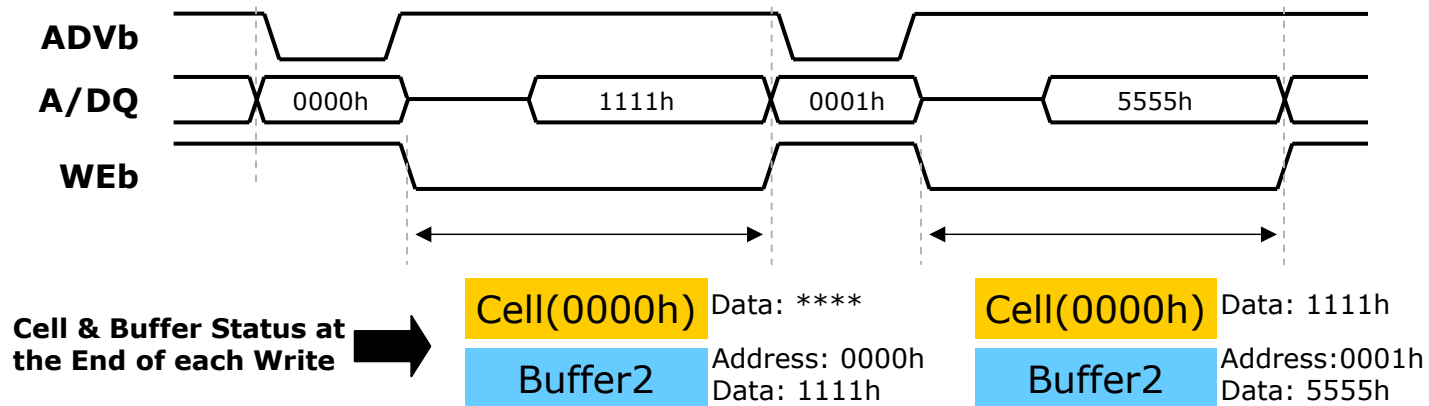


* UtRAM writes the current data directly in the cell during current write cycle.

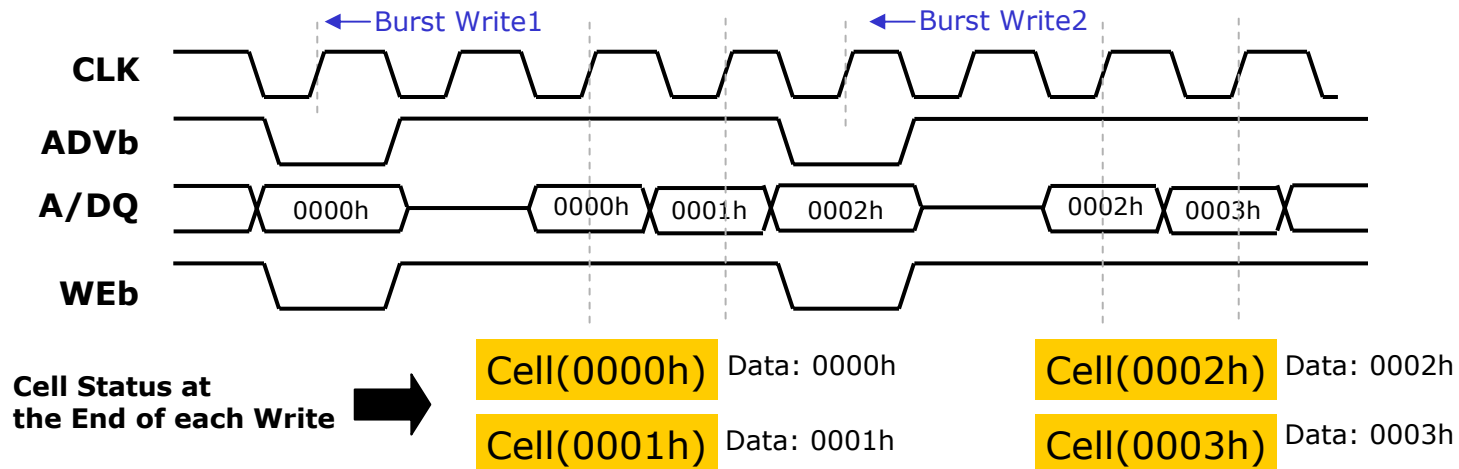
* UtRAM always accesses 'cell' when any address is input for Read.

UtRAM Write Example

Asynch Write



Synch Write



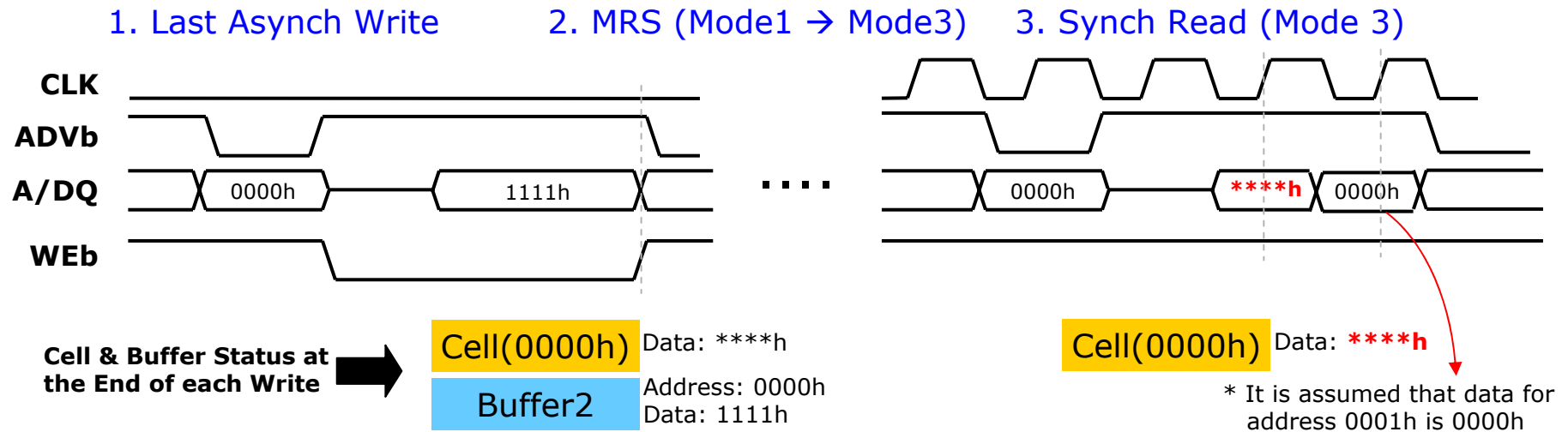
Write Mode & Mode Change

Mode Change Rule

- * UtRAM has 3 operating mode
 - Mode 1 : Asynch. Read / Asynch. Write
 - Mode 2: Synch Read / Asynch. Write
 - Mode 3: Synch Read / Synch. Write
- * Different Write schematic between Asynch write & Synch Write makes the Mode change Rule to be needed.
- * Mode1 to Mode2: no rule ← Write method for Mode 1 & Mode2 is Asynchronous Write.
- * Mode1(2) to Mode3: 1 Dummy Write is necessary to any address with any data right before the 'Mode3 to Mode1(or2) change'
- * Mode3 to Mode1(2): 1 Dummy Write is necessary to the same address with same data which are used right before the 'Mode1(2) to Mode3 change'

Write Mode & Mode Change

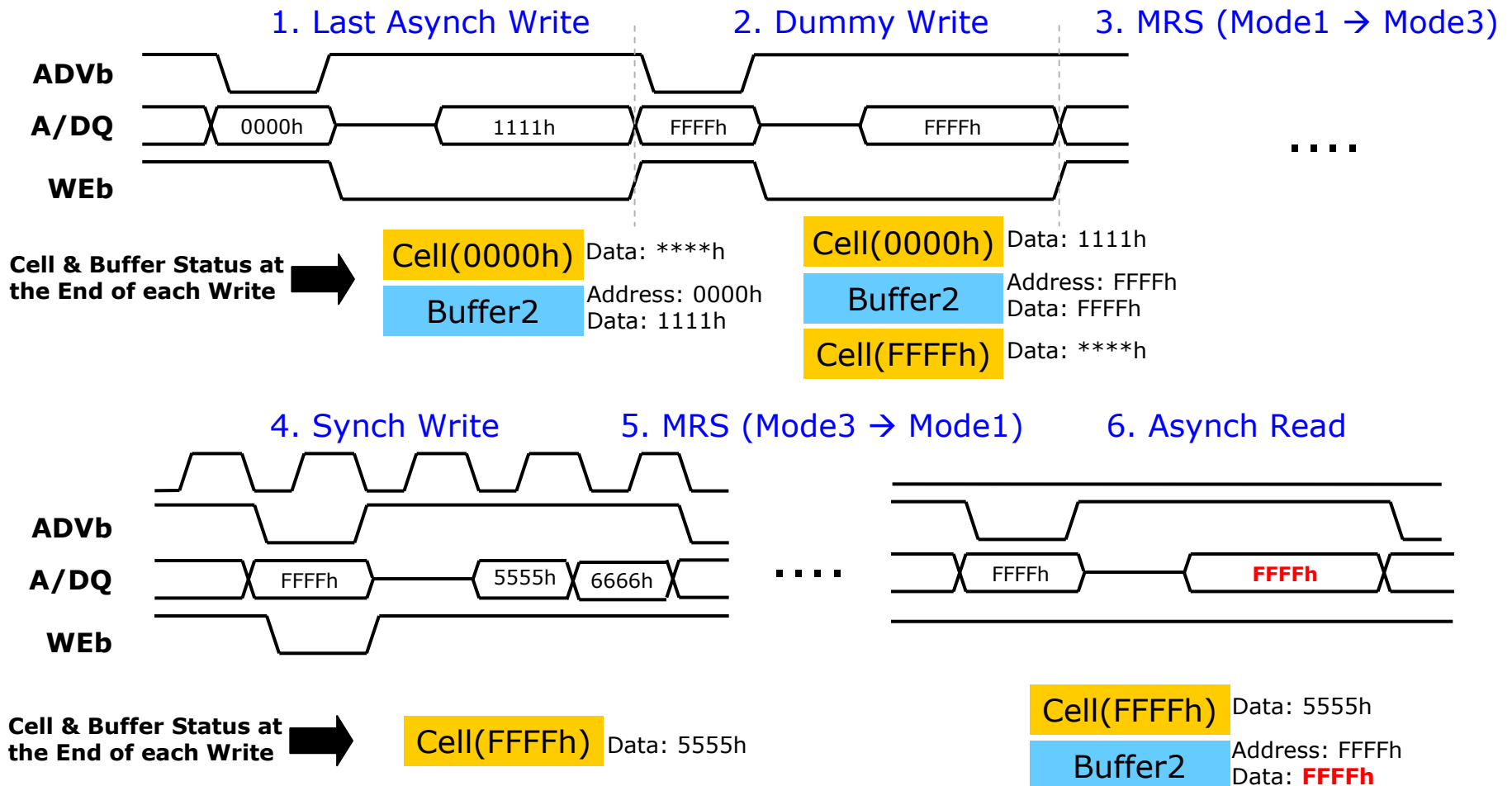
Mode 1 (or Mode 2) → Mode3



1. Last write data(1111h) stores in Buffer2.
 2. Implements MRS and change the mode from '1' to '3'
 3. Output data is ****h instead of 1111h when the address 0000h is accessed because cell(0000h) is directly accessed in Mode 3 while the actual data is in the Buffer2
- **"Dummy write"** to transfer the data in the Buffer2 to Cell(0000h) is necessary before implementing MRS to change the mode from '1(or2)' to '3'

Write Mode & Mode Change

Mode 3 → Mode 1 (or Mode 2)



Write Mode & Mode Change

Mode 3 → Mode 1 (or Mode 2)

1. Last write data(1111h) stores in Buffer2.
 2. Dummy Write to 'address FFFFh' transfers the last 'data(1111h)' to the 'cell(0000h)' and Buffer2 stores 'address FFFFh' & 'data (FFFFh)'
 3. MRS is implemented to change the mode from '3' to '1(or2)'
 4. Write is implemented during mode3 and the data(5555h) is written into cell(FFFFh).
 5. MRS is implemented to change the mode from '3' to '1(or2)'
 6. Output data is FFFFh instead of 5555h when the 'address FFFFh' is input because, in Mode1 (or Mode2), UtRAM is supposed to access the buffer2 when the lastly input address when it was Mode1 is input.
- "**Dummy write**" is necessary to the same address with same data which are used right before the 'Mode1(2) to Mode3 change' to make the the address & the data in the cell & Buffer2 to be the same.