

Address Matching in 8Mb/16Mb/32Mb SGRAM (for backward compatibility among SGRAMs)

Abstract

Many of SGRAM users are confused when they are to match Bank Select Address and Auto Precharge pin among the various density of SGRAMs(8Mb/16Mb/32Mb) and to keep backward compatibility, because the name or number of their address are different each other. However, SGRAMs can keep the backward compatibility even though they have different pin-outs. This application note explains how these SGRAMs keeps their backward compatibility.

Address Translation Table of SGRAMs

All of SGRAMs use 100pin QFP package, but address names of pin 29, 30 and 51 are different each other. However, the physical placements of Bank Select Address and Auto Precharge pin are same. For the detailed pin name information, refer to the table 1.

Table 1: Address Translation Table of SGRAMs

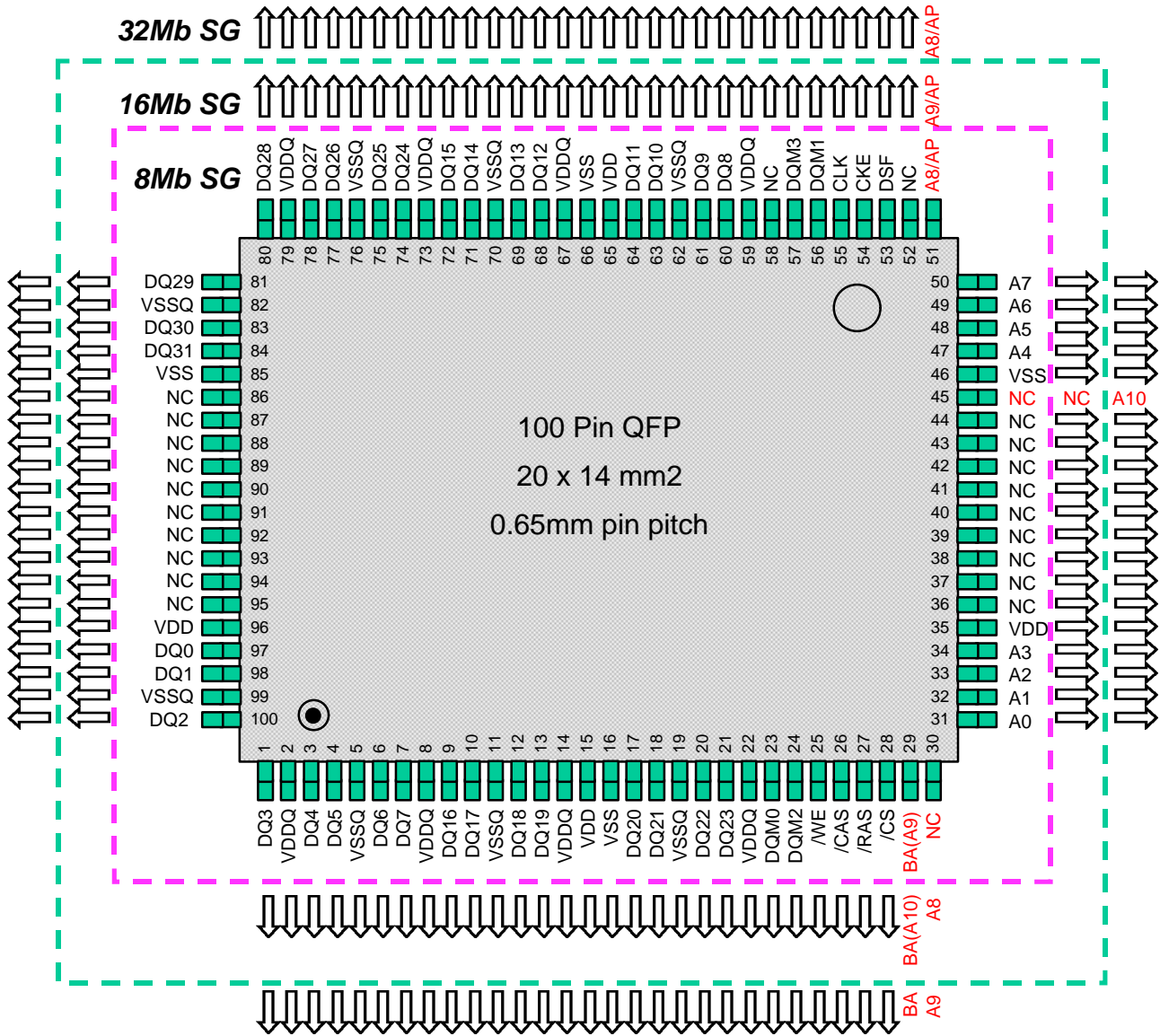
Function	256K x 32	512K x 32	1M x 32	Pin-out
Bank Address	BA(A9)	BA(A10)	BA	29*
Auto Precharge	A8/AP	A9/AP	A8/AP	51*
Row Address	A0~A8	A0~A9	A0~A10	
Col. Address	A0~A7	A0~A7	A0~A7	

* The functionality of this pin is same regardless of pin name.

Board design to use same foot print all, 8Mb, 16Mb and 32Mb SGRAM.

All of SGRAMs use same package type, 100pin QFP(PQFP, TQFP, LQFP), which can be mounted on the same foot print of PCB. Basically, all SGRAMs use same pin-outs except adding one row address whenever the memory size is doubled. In 8Mb and 16Mb SGRAM case, the MSB address is used as Bank Select Address (respectively BA(A9), BA(A10)) and the next of MSB address is used as Auto Precharge address (respectively A9/AP, A8/AP). However, for backward compatibility, the physical position of them are assigned in same pin. If we assume one board which has 100pin QFP foot print for 8Mb SGRAM, one pin, regardless of the name at controller, is connected to pin 51 of 8Mb SGRAM. The name of pin 51 is A8/AP on 8Mb SGRAM. If he replace the 8Mb with a 16Mb device, the same pin at controller will be connected to A9/AP of the 16Mb SGRAM. It does not matter the row addresses being swapped. But in fact, asserting a same command (function) at a same pin is more important in the design. Hence, controller makers and board designers do not have to concern compatibility issue when they interchange 8M SGRAM with 16Mb SGRAM, as long as they keep the same command (function) at the same pin.

Figure 1: Pin Assignment of 100pin QFP of SGRAMs



Application Review (Graphic board design keeping compatibility)

A graphic subsystem may solder SGRAMs on a board or use SODIMM for graphic memory. Sometimes, they may solder SGRAMs on a board and extend the graphic memory size using SODIMM. That means there is a possibility of any kind of mixture with 8Mb, 16Mb and 32Mb SGRAM on a system and nobody knows which combination end user uses.

How to keep the interchangeability between different densities

For the customer who wants to keep interchangeability between different densities (8Mbit/16Mbit/32Mbit) without a design change of existing controller, we recommend him/her not to use single bit write mode which is set by A9 during MRS cycle. By doing this, our customer can be free from any confusion which might be brought up when they attempt to replace lower density sgram with higher density sgram.

Let's take an example with the pin#51 for customers' clear understanding though this interchangeability related concern seems to be raised quite less because customers seldom use single bit write function, In case of 16M SGRAM, this pin#51 is A9 which is used for WBL select during MRS cycle and can be either "0" or "1". On the other hand, in case of 8MSG/32MSG, this pin is A8 which is used for the test mode select and should be set to "0" during MRS cycle. To satisfy both cases' requirement, this pin # 51 should be set to "0". Refer to the below table for further information.

Table 2 : Pin status during MRS Cycle

Pin Number	Pin # 29	Pin # 30	Pin # 51	Comment
256Kx32 SGRAM	A9	NC	A8	Addr function 0 1
512Kx32 SGRAM	BA	A8	A9	A8 TM default illegal
1Mx32 SGRAM	BA	A9	A8	A9 BT burst single bit
				BA RFU default illegal
Truth Table	0	0	0	All are fine
	0	0	1	16MSG : SBW* & 8M/32MSG : illegal
	0	1	0	32MSG : SBW* & 16MSG : illegal
	0	1	1	All are illegal
	1	0	0	8MSG : SBW* & 16M/32MSG : illegal
	1	0	1	All are illegal
	1	1	0	All are illegal
	1	1	1	All are illegal

* SBW : Single bit write

How to use different densities on one board with minimal design change

Some customers would rather use the higher density memory product due to the availability in present market than they really need it. In that case, they use the half density out of the whole density placed in the system and have to pay a special attention for normal operation.

In case of using 16M SG instead of 8M SG or 32M SG instead of 16M SG in same system, one address pin may be needless for half density operation and this pin has to be dealt with special handling. The additional address pins must be tied to the ground on the PCB because it may cause an abnormal operation when left floated.

Bring up an issue

On 100pin QFP, AP and BA pins are connected to pin 51 and 29 respectively regardless of different address name on 8Mb, 16Mb and 32Mb SGRAM component. But JEDEC SODIMM standard defines just the address number of each pin. 8Mb based SODIMM is using the same address name as JEDEC standard. If we want to keep the compatibility on module with JEDEC definition, component address names of 16Mb SGRAM have to be changed. Otherwise, in the same manner, module address names have to be changed. Notice, all these are just name issues, not physical issues.

16Mb based Module Proposal to keep the backward compatibility with 8Mb SGRAM based SODIMM.

If we change the names of pin 80,81 and 82 on 16Mb SGRAM based SODIMM as table 2, we can use 8Mb, 16Mb and 32Mb SGRAM on a board with a very basic assumption that graphic controller can deal with the different address names. Actually, controller must understand the different address mapping of 8Mb, 16Mb and 32Mb SGRAM to support all density. Therefore, Samsung proposed 16Mb/32Mb SGRAM based SODIMM pin names as table 2. For more detailed information, refer to Figure 2.

Table 2: Address Translation Table of SGRAM SODIMM

Old JEDEC		256K x32 based		512K x 32 based		1M x 32 based	
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
92	A0	92	A0	92	A0	92	A0
91	A1	91	A1	91	A1	91	A1
90	A2	90	A2	90	A2	90	A2
89	A3	89	A3	89	A3	89	A3
88	A4	88	A4	88	A4	88	A4
87	A5	87	A5	87	A5	87	A5
84	A6	84	A6	84	A6	84	A6
83	A7	83	A7	83	A7	83	A7
82	A8	82	A8/AP	82	A9/AP	82	A8/AP
81	A9	81	BA(A9)	81	BA(A10)	81	BA
80	A10	80	N.C	80	A8	80	A9
79	A11/RSVD	79	N.C	79	N.C	79	A10

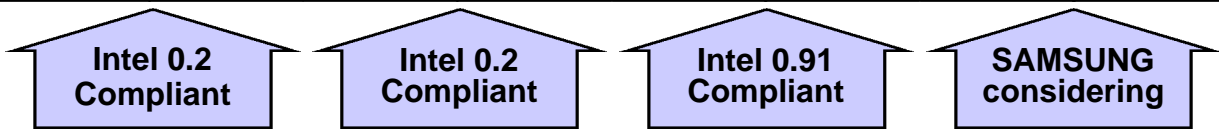


Figure 2: Signal connection diagram

