

**How to keep the interchangeability
among different density SGRAMs(8/16/32MSG)**

How to keep the interchangeability between different densities

For the customer who wants to keep interchangeability between different densities(8Mbit/16Mbit/32Mbit) without a design change of existing controller, we recommend him/her not to use single bit write mode which is set by A9 during MRS cycle. By doing this, our customer can be free from any confusion which might be brought up when they attempt to replace lower density sgram with higher density sgram.

Let's take an example with the pin#51 for customers' clear understanding though this interchangeability related concern seems to be raised quite less because customers seldom use single bit write function, In case of 16M SGRAM, this pin#51 is A9 which is used for WBL select during MRS cycle and can be either "0" or "1". On the other hand, in case of 8MSG/32MSG, this pin is A8 which is used for the test mode select and should be set to "0" during MRS cycle. To satisfy both cases' requirement, this pin # 51 should be set to "0". Refer to the below table for further information.

Table 2 : Pin status during MRS Cycle

Pin Number	Pin # 29	Pin # 30	Pin # 51	Comment
256Kx32 SGRAM	A9	NC	A8	Addr function 0 1
512Kx32 SGRAM	BA	A8	A9	A8 TM default illegal
1Mx32 SGRAM	BA	A9	A8	A9 BT burst single bit BA RFU default illegal
Truth Table	0	0	0	All are fine
	0	0	1	16MSG : SBW* & 8M/32MSG : illegal
	0	1	0	32MSG : SBW* & 16MSG : illegal
	0	1	1	All are illegal
	1	0	0	8MSG : SBW* & 16M/32MSG : illegal
	1	0	1	All are illegal
	1	1	0	All are illegal
	1	1	1	All are illegal

* SBW : Single bit write

How to use different densities on one board with minimal design change

Some customers would rather use the higher density memory product due to the availability in present market than they really need it. In that case, they use the half density out of the whole density placed in the system and have to pay a special attention for normal operation.

In case of using 16M SG instead of 8M SG or 32M SG instead of 16M SG in same system, one address pin may be needless for half density operation and this pin has to be dealt with special handling. The additional address pins must be tied to the ground on the PCB because it may cause an abnormal operation when left floated.

Figure 1: Pin Assignment of 100pin QFP of SGRAMs

