

# DDR2 ODT Control

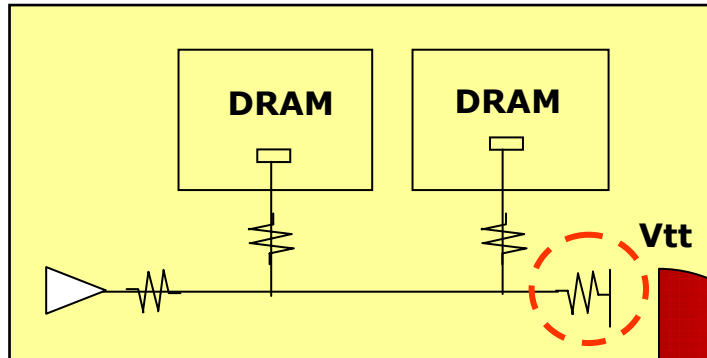
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**MEMORY DIVISION  
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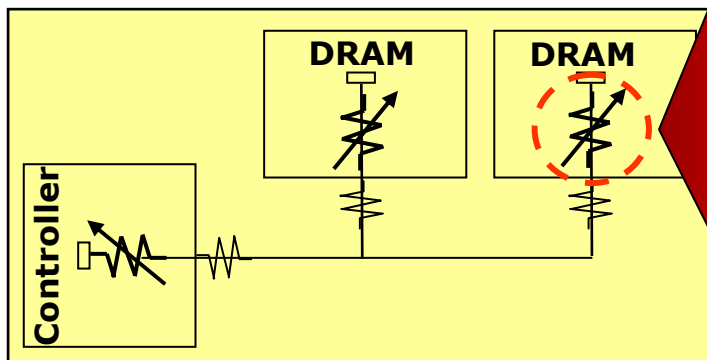
# DDR2 On Die Termination (ODT)

Motherboard Termination (MBT)

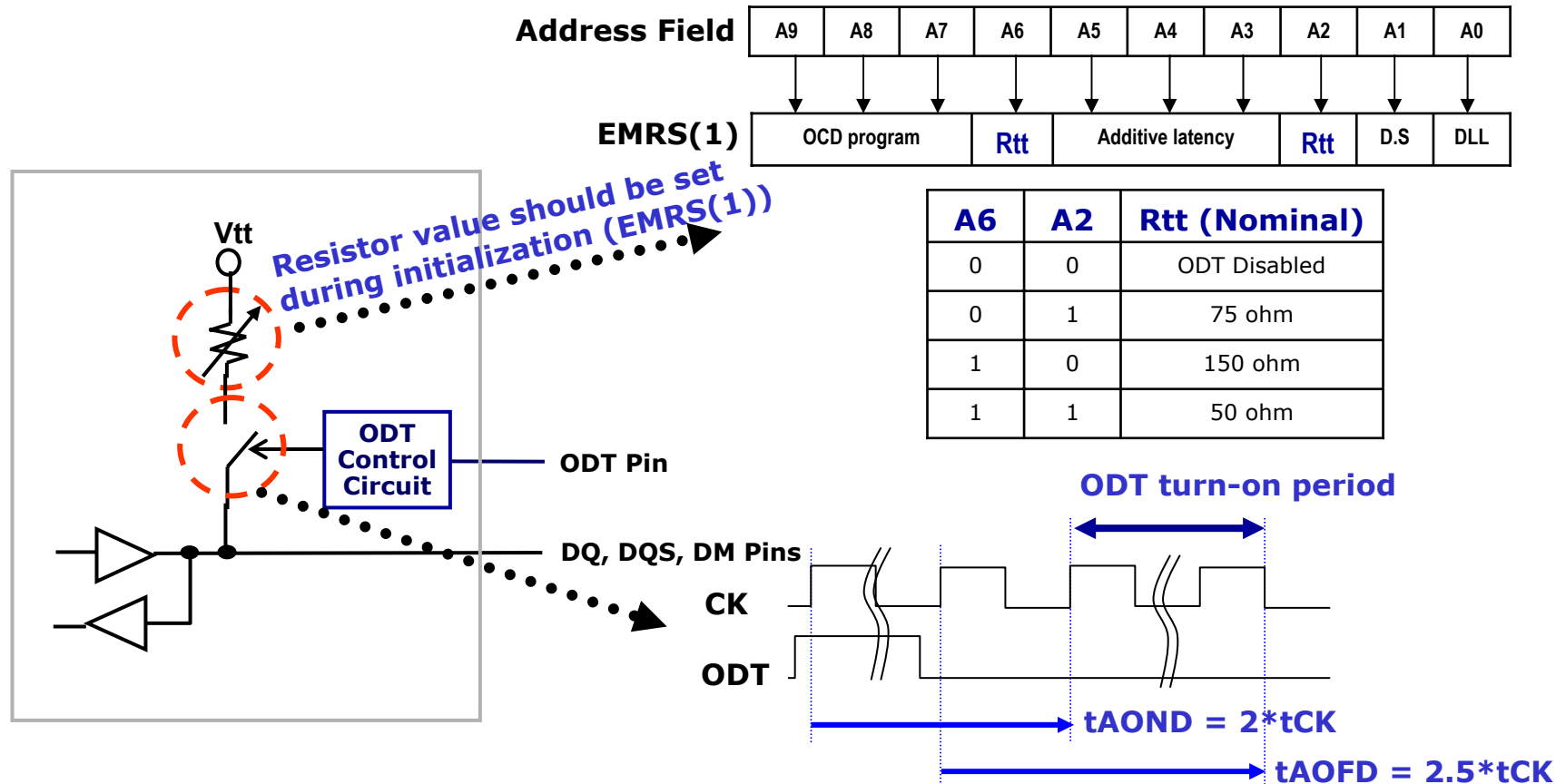


- ❑ On board termination resistance is integrated inside of DRAM

DDR2 On Die Termination (ODT)

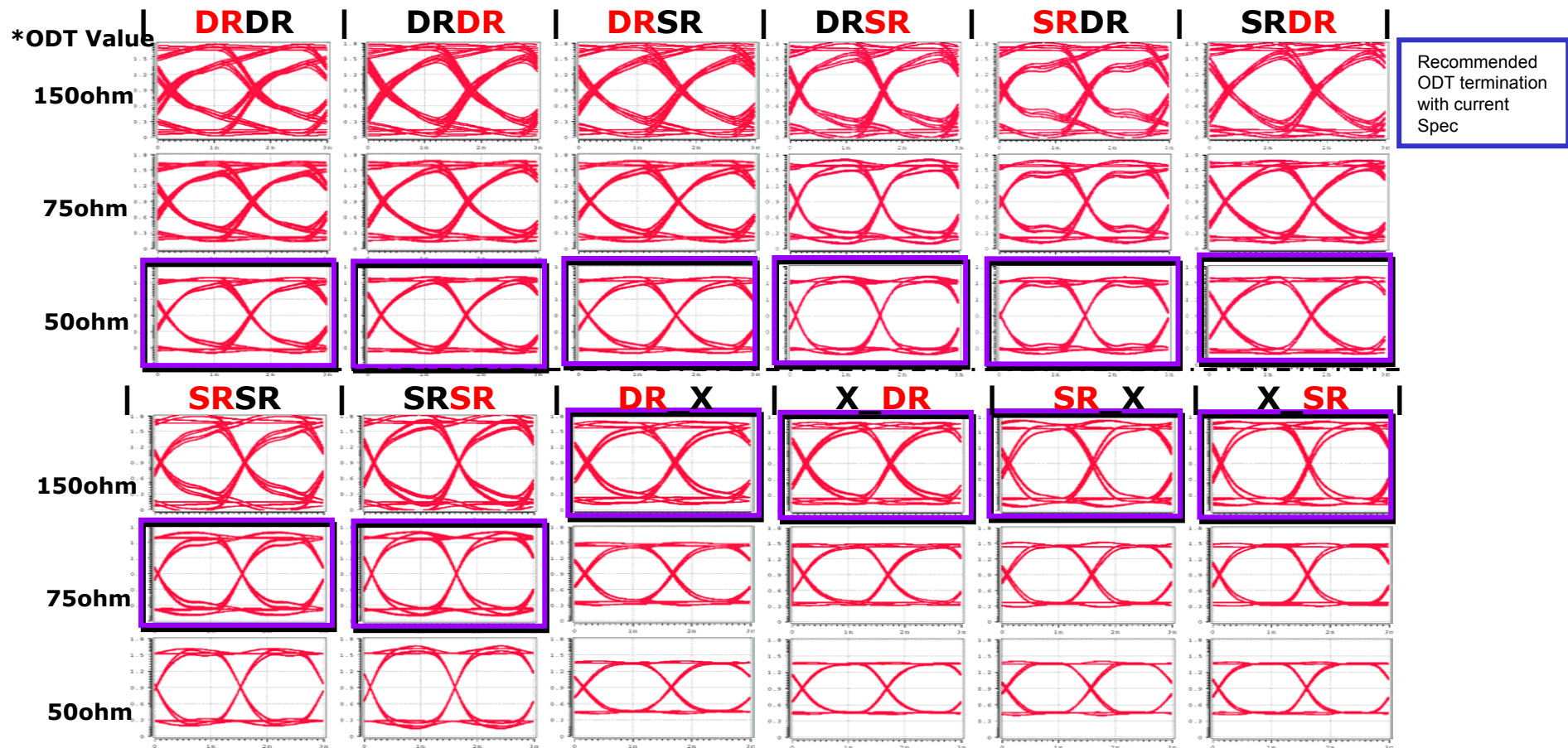


# ODT Value Selection & On/Off Control



- ❑ ODT value should be determined during power-up by EMRS
- ❑ ODT turn on/off is controlled by ODT pin
- ❑ One ODT control pin per DRAM : Turn-on or Turn-off control
- ❑ Two ODT control pins per DIMM to support rank by rank control, *but in most application, one ODT pin per slot is being used*

# ODT Case Study @DDR2-667 Writes



- ❑ For two slot population, 50ohm seems to be better than 75ohm in terms of signal integrity
- ❑ For one slot population, 150ohm seems OK

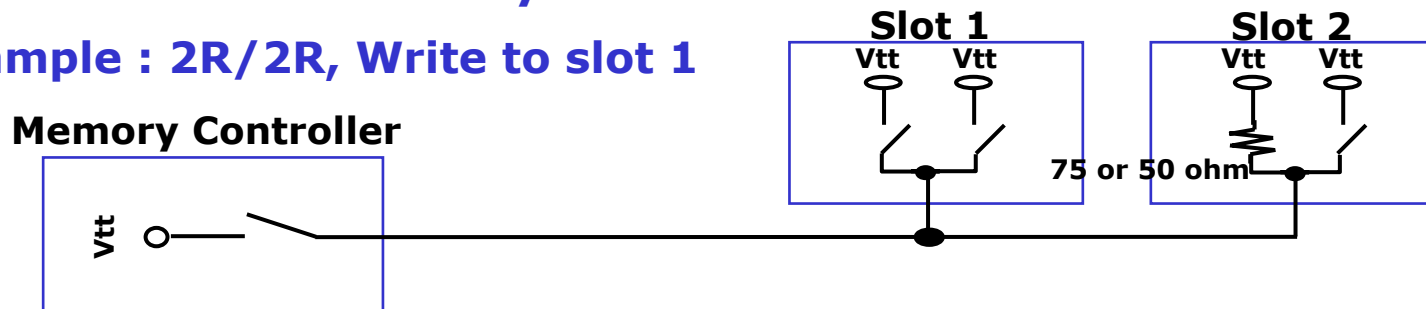
# Recommended ODT Control - Writes

## Termination Matrix for Writes to DRAM

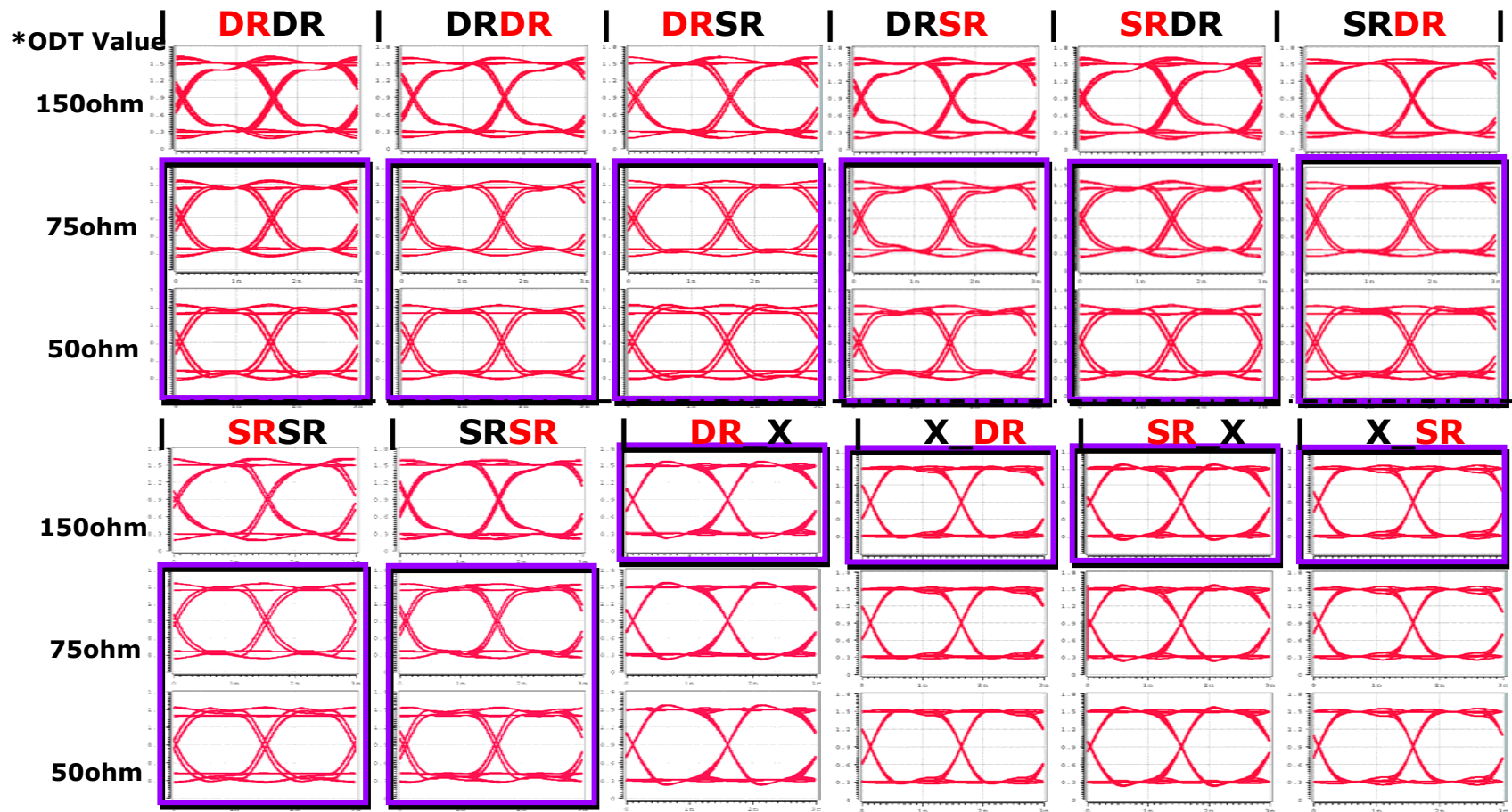
Configuration	Write to	Target DQ ODT Resistance $R_{TT}$				
		Controller	Module in slot 1		Module in slot 2	
			Rank 1	Rank 2	Rank 1	Rank 2
2R/2R	Slot 1	Infinite	Infinite	Infinite	75 or 50 ohm*	Infinite
	Slot 2	Infinite	75 or 50 ohm*	Infinite	Infinite	Infinite
2R/1R	Slot 1	Infinite	Infinite	Infinite	75 or 50 ohm*	Unpopulated
	Slot 2	Infinite	75 or 50 ohm*	Infinite	Infinite	Unpopulated
1R/2R	Slot 1	Infinite	Infinite	Unpopulated	75 or 50 ohm*	Infinite
	Slot 2	Infinite	75 or 50 ohm*	Unpopulated	Infinite	Infinite
1R/1R	Slot 1	Infinite	Infinite	Unpopulated	75 or 50 ohm*	Unpopulated
	Slot 2	Infinite	75 or 50 ohm*	Unpopulated	Infinite	Unpopulated
2R/Empty	Slot 1	Infinite	150 ohm	Infinite	Unpopulated	Unpopulated
Empty/2R	Slot 2	Infinite	Unpopulated	Unpopulated	150 ohm	Infinite
1R/Empty	Slot 1	Infinite	150 ohm	Unpopulated	Unpopulated	Unpopulated
Empty/1R	Slot 2	Infinite	Unpopulated	Unpopulated	150 ohm	Unpopulated

ODT on a controller always turned-off

Example : 2R/2R, Write to slot 1



# ODT Case Study @DDR2-667 Reads



- ❑ For two slot population, either 75ohm or 50ohm could be OK even at DDR2-667 operation
  - 50 ohm option has been added for DDR2-667/800, but it does not help on reads that much
- ❑ For one slot population, 150ohm seems OK

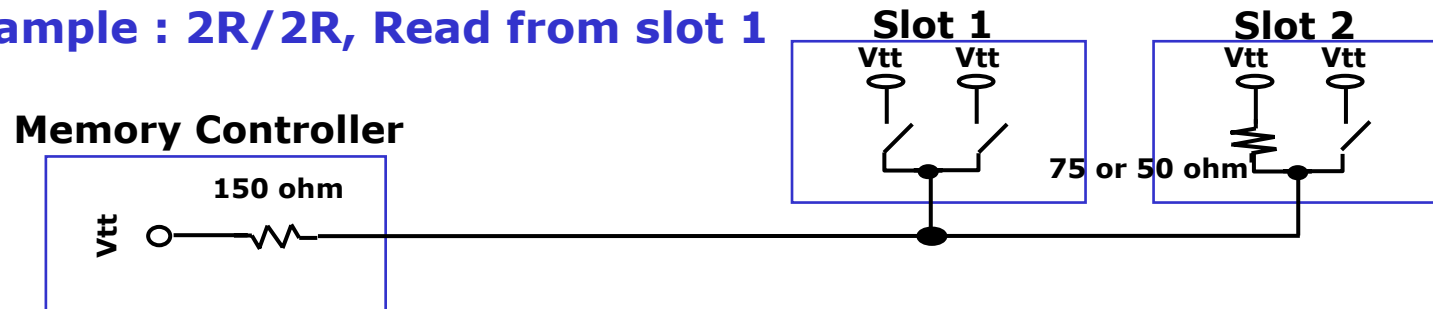
# Recommended ODT Control - Reads

## Termination Matrix for Reads from DRAM

Configuration	Read from	Target DQ ODT Resistance $R_{TT}$				
		Controller	Module in slot 1		Module in slot 2	
			Rank 1	Rank 2	Rank 1	Rank 2
2R/2R	Slot 1	150 ohm	Infinite	Infinite	75 or 50 ohm*	Infinite
	Slot 2	150 ohm	75 or 50 ohm*	Infinite	Infinite	Infinite
2R/1R	Slot 1	150 ohm	Infinite	Infinite	75 or 50 ohm*	Unpopulated
	Slot 2	150 ohm	75 or 50 ohm*	Infinite	Infinite	Unpopulated
1R/2R	Slot 1	150 ohm	Infinite	Unpopulated	75 or 50 ohm*	Infinite
	Slot 2	150 ohm	75 or 50 ohm*	Unpopulated	Infinite	Infinite
1R/1R	Slot 1	150 ohm	Infinite	Unpopulated	75 or 50 ohm*	Unpopulated
	Slot 2	150 ohm	75 or 50 ohm*	Unpopulated	Infinite	Unpopulated
2R/Empty	Slot 1	75 ohm	Infinite	Infinite	Unpopulated	Unpopulated
Empty/2R	Slot 2	75 ohm	Unpopulated	Unpopulated	Infinite	Infinite
1R/Empty	Slot 1	75 ohm	Infinite	Unpopulated	Unpopulated	Unpopulated
Empty/1R	Slot 2	75 ohm	Unpopulated	Unpopulated	Infinite	Unpopulated

ODT on a controller always turned-on

Example : 2R/2R, Read from slot 1



# Summary - ODT Control

- ❑ **ODT value should be decided depending on channel environment and set during initialization sequence**
  - **For one slot/channel implementation, 150ohm seems OK**
  - **For two slots/channel implementation, ODT value need to be determined properly**
  - **For DDR2-400/533, 75ohm seems OK**  
**For DDR2-667 or higher, 50ohm is better than 75ohm**
  
- ❑ **ODT turn-on/off is controlled by ODT pin**
  
- ❑ **There are more possible termination methods, but not covered in this material**
  - **For example, 37.5 ohm termination is possible with both ODTs turned-on on a dual rank DIMM, which may result “better signal integrity, but relatively small voltage swing and more power consumption”**