Making higher density SDRAM with low power feature

Application Notes(August '04)

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Introduction

The important characteristic of cellular phone is the battery usage for power source. Cellular phone's size is getting smaller and smaller to reduce its weight, to carry it conveniently without increasing battery size. So the power consumption is the most critical point in cellular phone.

To support multimedia service, the performance is getting stronger and stronger. But the penalty for supporting multimedia with a cellular phone is a little critical due to its large power consumption; to support color display, to run a movie, to communicate with seeing caller's face and etc. To realize these kinds of multimedia service, higher density & higher speed is required.

How to make higher density SDRAM

Sometimes set-makers want higher density SDRAM than memory vendors can provide. Because users want more advanced multimedia services than expected. Normal way to make higher density SDRAM is combination of 2 pieces of SDRAM. For example, we can make 512Mb x32 SDRAM with 2 pieces of 256Mb SDRAM.

Case 1	Case 2	Case 3	Case 4
(512Mb x32) Monolithic	(256Mb x16) 2pieces	(256Mb x32) 2pieces	(256Mb x32) 2pieces
1/CS, 1CKE	1/CS, 1CKE	2/CS, 1CKE	2/CS, 2CKE

Table. 1 - 512Mb x32 SDRAM configuration.

Case 1 is monolithic 512Mb x32 SDRAM. With current process technology, the size of 512Mb x32 SDRAM is too big for MCP(Multi Chip Package) product. SDRAM's chip size is mainly concerned with design rule. Set-makers would not accept the chip size penalty. At this moment, case 1 is not available, so case 2, 3, 4 can be possible solution of 512Mb x32 SDRAM with MCP. The availability of each case except case 1 can be dependant on the chipset. SDRAM users should be aware of chipset's supportability.

Usage of different memory configuration

Memory configuration in each case is different. So connecting between chipset and SDRAM should be different.

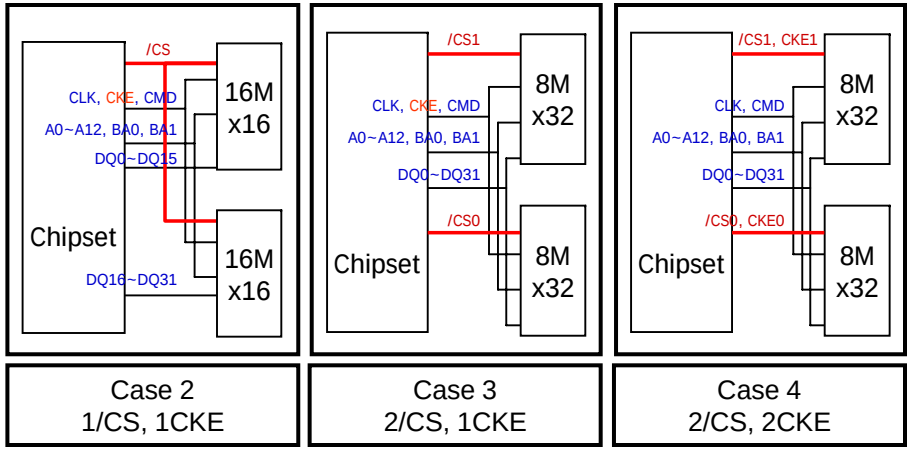

Figure. 1 - Connecting between chipst and SDRAM

Another concerning point is address mapping. In case 3 & 4 SDRAM is basically composed of 2 chips with 2/CS. Thus two chip's physical memory address can be discrete. But modern chipset has the function of MMU(Memory Management Unit), memory address can be read continuously. The last address of /CS0 and the first address of /CS1 are continuously mapped by MMU.

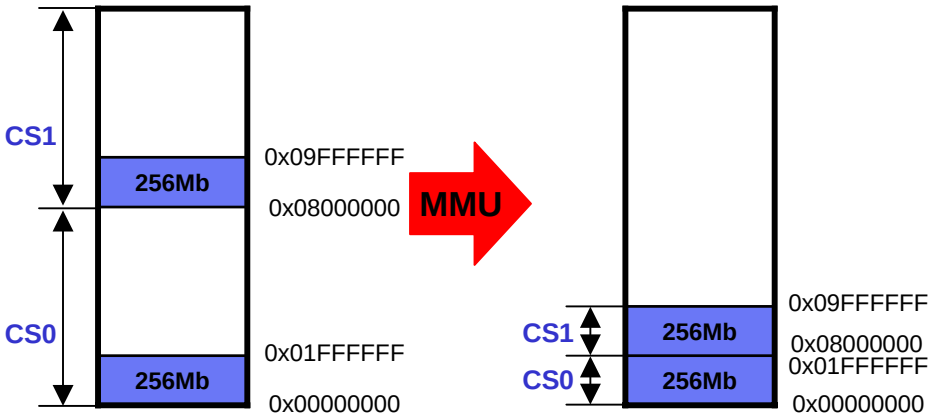

Figure. 2 - The Role of MMU (Memory Management Unit)

Power consumption Comparison among different memory solutions

When 2 chips are combined into the higher density memory, total power consumption would be different from case by case. The following table shows the parameter & test condition of DC characteristics of SDRAM.

Parameter	Symbol	Test Condition
Operating Current (One Bank Active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}(min)$ Io = 0 mA
Precharge Standby Current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), tcc = 10ns
	I_{CC2PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞
Precharge Standby Current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 10ns Input signals are changed one time during 20ns
	I_{CC2NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable
Active Standby Current in power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), tcc = 10ns
	I_{CC3PS}	CKE & CLK ≤ V_{IL}(max), tcc = ∞
Active Standby Current in non power-down mode (One Bank Active)	I_{CC3N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), tcc = 10ns Input signals are changed one time during 20ns
	I_{CC3NS}	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), tcc = ∞ Input signals are stable
Operating Current (Burst Mode)	I_{CC4}	Io = 0 mA Page burst 4Banks Activated t_{CCD} = 2CLKs
Refresh Current	I_{CC5}	$t_{ARFC} \geq t_{ARFC}$(min)
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V

Table. 2 - DC Characteristics of SDRAM

Power consumption is related with SDRAM's status. When one chip is in active state, the other can be stand-by state or self refresh state according to /CS & CKE status. Refer to the Table.3 (Function Truth Table of SDRAM)

Current State	CKE (n-1)	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Action	Note
Idle	H	L	L	L	L	H	X	Enter Self Refresh	
Self Refresh	H	X	X	X	X	X	X	Exit Self Refresh --> Idle after t_{RC}/t_{SRFX} (ABI)	
	L	H	H	X	X	X	X	Exit Self Refresh --> Idle after t_{RC}/t_{SRFX} (ABI)	
	L	H	L	H	H	H	X	Exit Self Refresh --> Idle after t_{RC}/t_{SRFX} (ABI)	

Table. 3 - Function Truth Table (SDRAM)

Following table can explain power consumption comparison of these kinds of SDRAM easily. The definition of each parameter (ICC1, ICC2N, ICC4, ICC6) is on Table. 2

	Case 2	Case 3	Case 4
	(256Mb x16) x2	(256Mb x32) x2	(256Mb x32) x2
	1/CS, 1CKE	2/CS, 1CKE	2/CS, 2CKE
ICC1	1 x (2 x ICC1(x16))	0.65 x (ICC1(x32) + ICC2N(x32))	0.57 x (ICC1(x32) + ICC6(x32))
ICC4	1 x (2 x ICC4(x16))	0.70 x (ICC4(x32) + ICC2N(x32))	0.67 x (ICC4(x32) + ICC6(x32))
ICC6	1 x (2 x ICC6(x16))	1 x (2 x ICC6(x32))	1 x (2 x ICC6(x32))

Table. 4 - SDRAM(x32) Power Consumption Comparison

This table shows there is power consumption difference among 3 cases. Regarding operating current (ICC1, ICC4), there is dramatic power consumption reduction through Case 3 & 4. In self refresh current(ICC6), there is no current difference among case 2,3,4. It means we can reduce operating current by using 2/CS memory solution.

In power consumption point of view, case 4 is the best solution. So if there is no chipset that can support 2/CS & 2CKE, Case 3 is proper solution.

Conclusion

The more multimedia service is supported, the higher density and the lower power consumption in memory would be needed. We should consider low power feature when making high density SDRAM.

Modern cellular phone's functions are getting complicated more and more. (Movie service, Digital Multimedia Broadcasting service, Network game service…) This kinds of services require lots of power in operating condition within fixed time. Cellular phone's state can be stand-by or operating state. The ability of power management in operating state is the key for mobile multimedia application.

Currently when making high density memory with combining 2 chips of SDRAM, 2/CS solution is the best in the operating power consumption point of view.

For more information

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