

Application Note

PC3200 DIMM(DDR400) SPD Program

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Memory division

PC3200 DIMM SPD Byte# description

- DDR Module SPD Description(JEDEC Standard)

Byte #	Function described
9	DDR SDRAM cycle time at Maximum Supported CAS latency(CL), CL=X
10	DDR SDRAM access time from clock at CL=X
23	DDR SDRAM cycle time at CL=X-0.5
24	DDR SDRAM access time from clock at CL=X-0.5
25	DDR SDRAM cycle time at CAS latency=X-1
26	DDR SDRAM access time from clock at CL=X-1

*CL: CAS# Latency

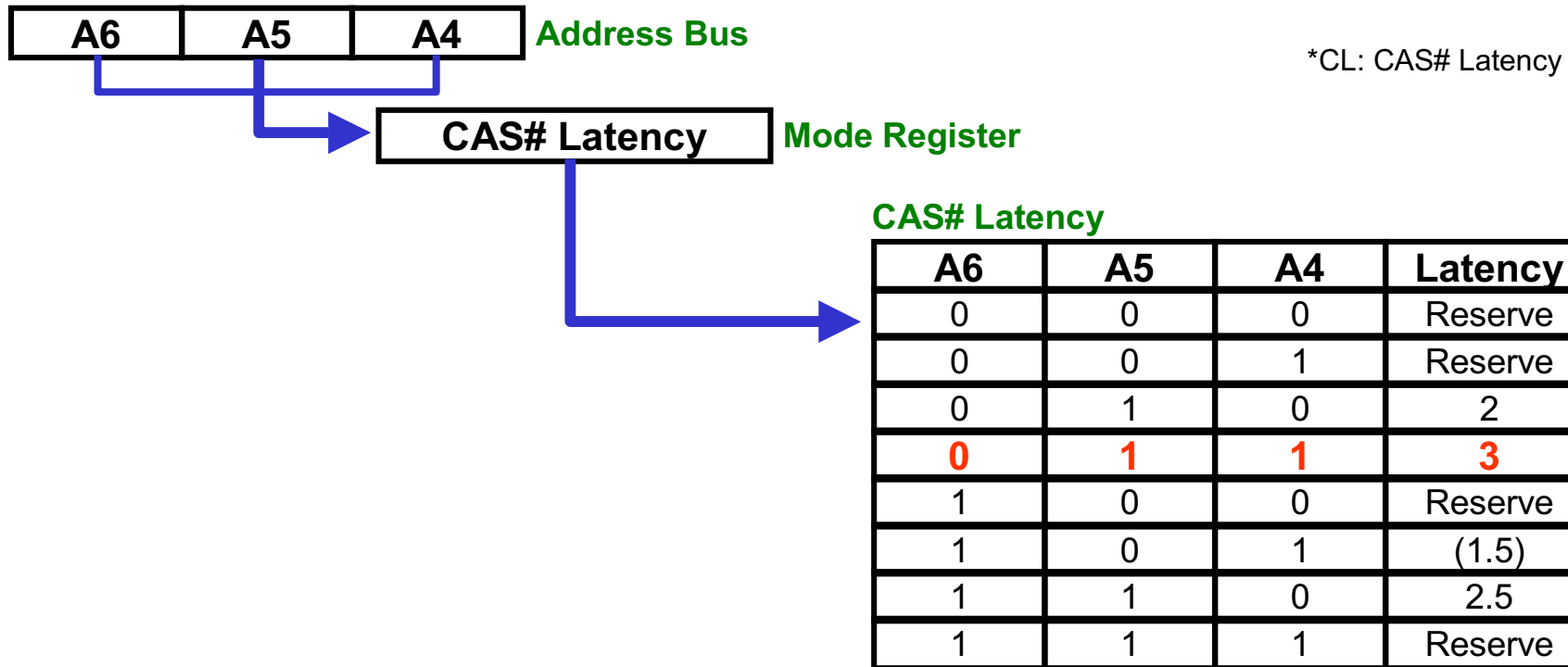
- CL="X" of Byte 9 means the highest CAS# Latency. So, CL="X" of DDR400 Module is "CL=3"

- DDR200/266/333 vs DDR400 Module SPD Description Comparison

Byte #	DDR200/266/333	DDR400
	Function described	Function described
9	DDR SDRAM cycle time at CAS latency=2.5	DDR SDRAM cycle time at CAS latency=3
10	DDR SDRAM access time from clock at CL=2.5	DDR SDRAM access time from clock at CL=3
23	DDR SDRAM cycle time at CAS latency=2.0	DDR SDRAM cycle time at CAS latency=2.5
24	DDR SDRAM access time from clock at CL=2.0	DDR SDRAM access time from clock at CL=2.5
25	DDR SDRAM cycle time at CAS latency=1.5	DDR SDRAM cycle time at CAS latency=2.0
26	DDR SDRAM access time from clock at CL=1.5	DDR SDRAM access time from clock at CL=2.0

- When System makers set BIOS based on SPD Program, please keep in mind the flexible SPD Byte # descriptions

MRS Set(CAS# Latency) of PC3200 DIMM



- The mode register stores the data for CAS# Latency of DDR SDRAM and MRS address bus for CAS# latency uses A4~A6.
- To implement CAS Latency=3, A4 & A5 must be assigned to “High” and A6 to “Low”.
- Only CAS# Latency=3 is supported to PC3200 DIMM.