
Program Method of NOR Flash

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Preliminary

Samsung Electronics

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Purpose

This application note will guide you to variable method of NOR flash and performance comparison. This is helpful for mobile software engineer.

Definitions and Acronyms

Definitions and Acronyms	Description
VID	Voltage for Accelerated program (typical 9.0V)
Amax	Maximum address bit

References

- Samsung NOR Flash Data sheet



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1. Variable program method of NOR Flash.

Samsung NOR flash devices provide variable program method for manufacturer of mobile goods. Normally SLC type NOR flash provides Quadruple word program in factory mode, and MLC type NOR flash provides Writer buffer program in both user and factory mode.

Normal Program (Both SLC & MLC)

NOR flash can be programmed in units of a word by using normal program method. Programming is writing 0's into the memory array by executing the Internal Program Routine. In order to perform the Internal Program Routine, a four-cycle command sequence is necessary. The first two cycles are unlock cycles. The third cycle is assigned for the program setup command. In the last cycle, the address of the memory location and the data to be programmed at that location are written. The device automatically generates adequate program pulses and verifies the programmed cell margin by the Internal Program Routine. During the execution of the Routine, the system is not required to provide further controls or timings. During the Internal Program Routine, commands written to the device will be ignored. Note that a hardware reset during a program operation will cause data corruption at the corresponding location.

Accelerated Program (Both SLC & MLC)

The device provides accelerated program operations through the Vpp input. Using this mode, faster manufacturing throughput at the factory is possible. When VID is asserted on the Vpp input, the device automatically enters the Unlock Bypass mode, temporarily unprotects any protected blocks, and uses the higher voltage on the input to reduce the time required for program operations. In accelerated program mode, the system would use a two-cycle program command sequence for only a word program. By removing VID returns the device to normal operation mode.

Note that Read While Accelerated Program (Erase) and Program suspend (Erase suspend) mode are not guaranteed in MLC devices.

Quadruple word accelerated program operation (SLC Only)

Quadruple word accelerated program operation allows the system write to a maximum of 4 words in one programming operation. As well as Single word accelerated program, the system would use five-cycle program sequence (One-cycle (XXX - A5H) is for quadruple word program command, and four cycles are for program address and data). By using Quadruple

word accelerated program operation, only four words programming is possible, and each program address must have the same Amax-A2 address. The device automatically generates adequate program pulses and ignores other command after program command.

Note that Read while Quadruple word accelerated program is not guaranteed

Writer Buffer Programming (MLC only)

Write Buffer Programming allows the system write to a maximum of 32 or 64 words in one programming operation. This results in faster effective programming time than the standard programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the block address in which programming will occur. The fourth cycle writes the block address and the number of word locations, minus one, to be programmed. For example, if the system will program 19 unique address locations, then 12h should be written to the device. This tells the device how many write buffer addresses will be loaded with data. The number of locations to program cannot exceed the size of the write buffer or the operation will abort. The fifth cycle writes the first address location and data to be programmed. In case that the device supports maximum 32 words program in one programming operation, the write-buffer-page is selected by address bits Amax - A5 entered at fifth cycle. All subsequent address/data pairs must fall within the selected write-buffer-page, so that all subsequent addresses must have the same address bit Amax - A5 as those entered at fifth cycle. Write buffer locations may be loaded in any order.

Once the specified number of write buffer locations have been loaded, the system must then write the "Program Buffer to Flash" command at the block address. Any other command address/data combination aborts the Write Buffer Programming operation. The device then begins programming. Data polling should be used while monitoring the last address location loaded into the write buffer. DQ7, DQ6, DQ5, and DQ1 should be monitored to determine the device status during Write Buffer Programming. The write-buffer programming operation can be suspended using the standard program suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device is ready to execute the next command. Note also that an address location cannot be loaded more than once into the write-buffer-page.

Accelerated Write Buffer Programming (MLC Only)

The device provides accelerated Write Buffer Program operations through the Vpp input. Using this mode, faster manufacturing throughput at the factory is possible. When VID is asserted on the Vpp input, the device temporarily unprotects any protected blocks, and

uses the higher voltage on the input to reduce the time required for program operations. In accelerated Write Buffer Program mode, the system must enter "Write to Buffer" and "Program Buffer to Flash" command sequence to be same as them of normal Write Buffer Programming and only can reduce the program time. Note that the third cycle of "Write to Buffer Abort Reset" command sequence is required in an Accelerated mode.

Note that Read While Accelerated Write Buffer Program and Program suspend mode are not guaranteed.

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2. Performance comparison of each program method

Table below indicates program time for one unit word. (not one unit operation)

Program Method	Normal PGM MLC / SLC	Buffer PGM	Accelerated Buffer PGM	Quad Word PGM
Vpp Input Voltage	VCC	VCC	VID	VID
Mode	User	User	Factory	Factory
Applied Product	MLC / SLC	MLC	MLC	SLC
PGM Time (tPGM/Word)	80us/11.5us	10us	4us	1.6us

