
Synchronous (burst) mode register setting for NOR Application Note

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Preliminary

Samsung Electronics

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Purpose

This application note will show how to set synchronous (burst) read mode during NOR operation.

Both *Burst mode register* and *extended register* in NOR are related to synchronous read mode.

You can change the sync mode and sync type using by put any value into these register. This is helpful for NOR software engineers.

Definitions and Acronyms

Definitions and Acronyms	Description
SLC	Single Level Cell
MLC	Multi Level Cell
tIAA	Initial Access Time
AVD	Address Valid Input SIGNAL
CR	Configuration Register

References

NOR DATASHEET

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1. What is synchronous (burst) read mode?

The device is capable of continuous or preset length linear burst read operation. Burst read allows system to be able to fetch mass word data faster than a word of single read. For the burst mode, the system should determine how many clock cycles are desired for the initial word (tIAA) of each burst access and what mode of burst operation is desired using "Burst Mode Configuration Register" command sequence. In addition to, "Extended Configuration Register" should be used to entry synchronous mode regarding some of devices. It described below in more detail.

2. The latest NOR' line up

2.1 NOR' Line up is now available in 1Q, 2009

Part Name	Device Density	Version	SLC/ MLC
K8S6415ET(B)C	32Mbit	F die	SLC
K8S6415ET(B)C	64Mbit	C die	SLC
K8S2815ET(B)C	128Mbit	C die	SLC
K8F53(56)(57)15E(T/B/Z)A	256Mbit	A die	MLC
K8F09(12)15E(T/B/Z)A	512Mbit	A die	MLC

3. How to enter sync (synchronous) mode

There are two methods to enter the synchronous read mode.

3.1 Not using "Extended Configuration Register" *Called no option*

The synchronous (burst) mode will automatically start on the rising edge of the CLK Input when /AVD is low. If there are several CLKs in /AVD low, the last rising edge one is valid CLK.

3.2 Using "Extended Configuration Register" *Called Sync MRS Option*

The synchronous (burst) mode will automatically start on the rising edge of the CLK input when /AVD is low after Extended Mode Register Setting to A13=0, A12=1 (Case of 256, 512Mbit) and A12 =1 (Case of 32, 64, 128Mbit). If there are several CLKs in AVD low, the last rising edge one is valid CLK.

3.3 Product lists according to sync MRS option and no option

Options Density	Part Name	
	Sync MRS Option	No option
32Mbit	K8S3015ET(B)F K8S3315ET(B)F	K8S3115ET(B)F K8S3215ET(B)F
64Mbit	K8S6215ET(B)C K8S6515ET(B)C	K8S6315ET(B)C K8S6415ET(B)C
128Mbit	K8S2615ET(B)C K8S2915ET(B)C	K8S2715ET(B)C K8S2815ET(B)C
256Mbit	K8F5415ET(B)A K8F5515ET(B)A	K8F5315ET(B)A K8F5615ET(B)A K8F5715ET(B)A
512Mbit	K8F1015ET(B)A K8F1115ET(B)A	K8F0915ET(B)A K8F1215ET(B)A K8F1315ET(B)A

4. Burst Mode Configuration Register

4.1 Burst mode configuration register table for 256 / 512Mbit

Address Bit	Function	Settings(Binary)
A21	Output Driver Control	000 = setting 0
A20		001 = setting 1
A19		010 = setting 2 (Reserve) 011 = setting 3 (Reserve) 100 = setting 4 (default) 101 = setting 5 (Reserve) 110 = setting 6 (Reserve) 111 = setting 7
A18	RDY Active	0 = RDY active with data(default) 1 = RDY active one clock cycle before data
A17	Burst Read Mode	000 = Continuous(default)
A16		001 = 8-word linear with wrap
A15		010 = 16-word linear with wrap 011 ~ 111 = Reserve
A14	Programmable Wait State	0000 = Data is valid on the 4th active CLK edge after \overline{AVD} transition to VIH
A13		0001 = Data is valid on the 5th active CLK edge after \overline{AVD} transition to VIH (40Mhz*)
A12		0010 = Data is valid on the 6th active CLK edge after \overline{AVD} transition to VIH (50/54Mhz*)
A11		0011 = Data is valid on the 7th active CLK edge after \overline{AVD} transition to VIH (60/66Mhz*)
		0100 = Data is valid on the 8th active CLK edge after \overline{AVD} transition to VIH (70Mhz*)
		0101 = Data is valid on the 9th active CLK edge after \overline{AVD} transition to VIH (80/83Mhz*)
		0110 = Data is valid on the 10th active CLK edge after \overline{AVD} transition to VIH (90/100Mhz*)
	0111 = Data is valid on the 11th active CLK edge after \overline{AVD} transition to VIH (108/110Mhz*)	
	1000 = Data is valid on the 12th active CLK edge after \overline{AVD} transition to VIH (120Mhz*)	
	1001 = Data is valid on the 13th active CLK edge after \overline{AVD} transition to VIH (133Mhz*,default)	
	1010 = Data is valid on the 14th active CLK edge after \overline{AVD} transition to VIH	

4.2 Burst mode configuration register table for 32 / 64 / 128Mbit

Address Bit	Function	Settings(Binary)
A20	Output Driver Control	00 = Driver Multiplier : 1/3 01 = Driver Multiplier : 1/2 10 = Driver Multiplier : 1 (Default) 11 = Driver Multiplier : 1.5
A19		
A18	RDY Active	1 = RDY active one clock cycle before data 0 = RDY active with data(default)
A17	Burst Read Mode	000 = Continuous(default) 001 = 8-word linear with wrap 010 = 16-word linear with wrap 011 ~ 111 = Reserve
A16		
A15		
A14	Programmable Wait State	000 = Data is valid on the 4th active CLK edge after AVD transition to V _{IH} (50/54Mhz) 001 = Data is valid on the 5th active CLK edge after AVD transition to V _{IH} (60/66/70Mhz) 010 = Data is valid on the 6th active CLK edge after AVD transition to V _{IH} (80/83Mhz) 011 = Data is valid on the 7th active CLK edge after AVD transition to V _{IH} (90/100Mhz) 100 = Data is valid on the 8th active CLK edge after AVD transition to V _{IH} (108Mhz,default) 101 = Reserve 110 = Reserve 111 = Reserve
A13		
A12		

4.3 Set Burst mode configuration register command sequence

	No. of Cycle	1 ST Cycle	2 nd Cycle	3 rd Cycle
Address	3	0x555H	0x2AAH	CR + 0x555H
Data		0xAAH	0x55H	0xC0H

CR = Configuration Register setting value

Case of 256 / 512Mbit = A21 ~ A11 (Refer to 4.1).

Case of 32 / 64 / 128Mbit = A20 ~ A12 (Refer to 4.2)

Example code1 :

```
typedef volatile unsigned short UINT16;
/* Unlock command */
*( (UINT16 *) 0x555 ) = 0xAA;
*( (UINT16 *) 0x2AA ) = 0x55;
/* CR Value setting */
*( (UINT16 *)CR + 0x555 ) = 0xC0;
```

CR Value' Example

Device - 512Mbit, Output Drive Control [A21 :19] – 4, RDY Active [A18] – 1, Burst read mode [A17 :15] – 2, Programmable Wait State [A14 :11] – 3.

add	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10~A0
value	1	0	0	1	0	1	0	0	0	1	1	0x555

CR Value = 0x251B

```
*( (UINT16 *)0x251B ) = 0xC0;
```

5. Extended Configuration Register

5.1 Extended configuration register table for 256 / 512Mbit

Address Bit	Function	Settings(Binary)
A13	Read Mode	00 = Asynchronous Read Mode(default) 01 = Synchronous Burst Read Mode 10 ~ 11 = Reserve
A12		
A11	RDY Polarity	0 = RDY signal is active high (default) 1 = RDY signal is active low

5.2 Extended configuration register table for 16 / 32 / 128Mbit

Address Bit	Function	Settings(Binary)
A12	Read Mode	0 = Asynchronous Read Mode(default) 1 = Synchronous Burst Read Mode

Note : 16 ,32 and 128Mbit have no option about RDY Polarity, The only is set to active low.

5.3 Extended configuration register command sequence

	No. of Cycle	1 ST Cycle	2 nd Cycle	3 rd Cycle
Address	3	0x555H	0x2AAH	CR + 0x555H
Data		0xAAH	0x55H	0xC5H

CR = Configuration Register setting value

Case of 256 / 512Mbit = A13 ~ A11 (Refer to 5.1).

Case of 32 / 64 / 128Mbit = A12 (Refer to 5.2)

Example code1 :

```
typedef volatile unsigned short UINT16;
/* Unlock command */
*( (UINT16 *) 0x555 ) = 0xAA;
*( (UINT16 *) 0x2AA ) = 0x55;
/* CR Value setting */
*( (UINT16 *)CR + 0x555 ) = 0xC5;
```

CR Value' Example

Device - 512Mbit, Read mode [A13 : 12] – 1, RDY Polarity [A11] – 0.

Add	A13	A12	A11	A10~A0
value	0	1	0	0x555

CR Value = 0x15

```
*( (UINT16 *)0x15 ) = 0xC5;
```

6. The symptoms by improper value in sync mode

6.1 Asynchronous read operation is good, but synchronous only is problem.

6.2 The error is occurred after clock frequency is changing.

6.3 Some read data are misaligned when controller attempt to fetch read data.

Preliminary