

Rising & Falling Time of Output Pin with 90nm Technology Product

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Implementing a common layout

□ Introduce

This document describes the rising and falling time of output buffer by the output loading - 30pF (Spec range), 50pF, and 80pF (tester environment).

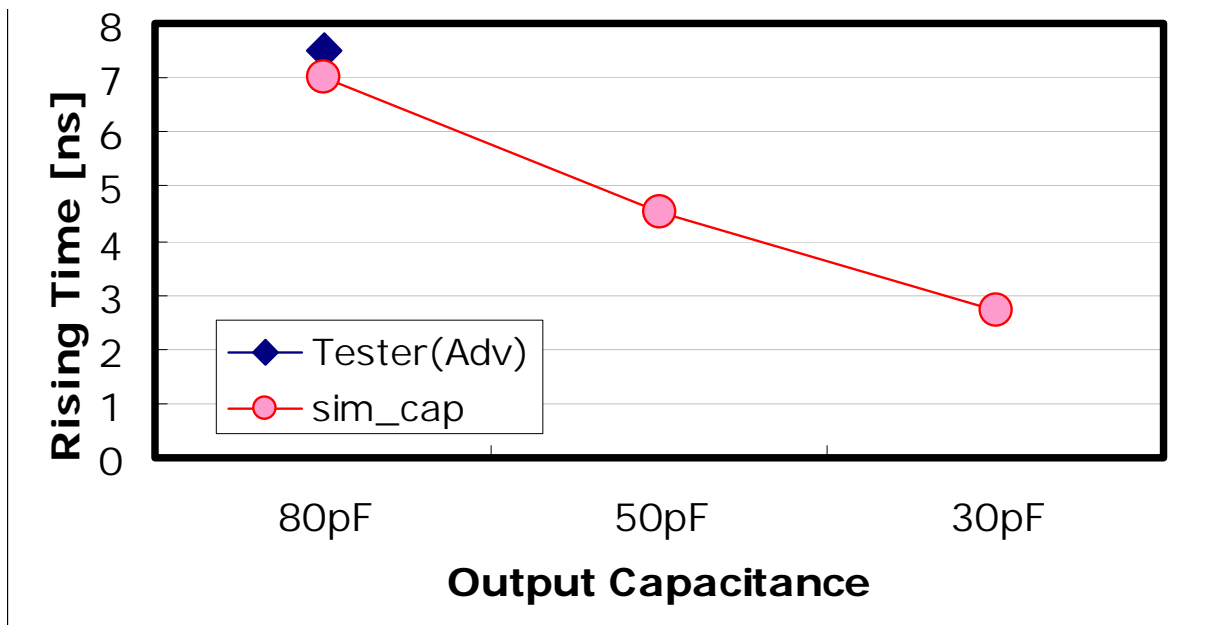
This value could be helpful to design user board with a specified timing set.

□ Definition of the Rising and Falling Time

1. We measured the rising and falling time with below condition.
 - . from 10% to 90% of slope and from 90% to 10%
2. The values at 30pF and 50pF are simulated and the value at 80pF is simulated and measured.
 - . Tester (Advantest T5371)
3. The Rising and Falling time of same technology is almost same - no depend on density - 256Mb, 128Mb, and 64Mb.
4. The measured and simulated value is with our 90nm products.

Rising & Falling Time of Outputs

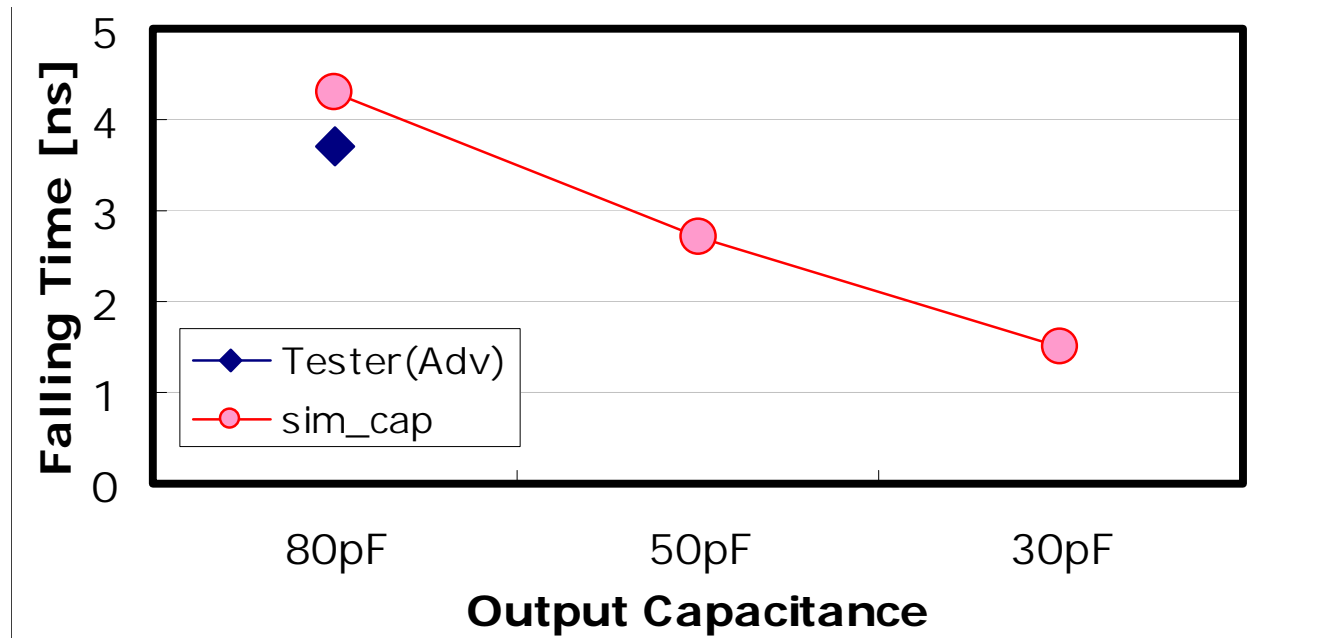
- **256Mb NOR Rising Time**(K8A5615ETA, K8A5615EBA)
(Test Condition : $V_{cc} = 1.7V$, Temp. = 85'C)



→ Because all of outputs have a same pad structure, the Simulation Value of rising slope have a same value.

Rising & Falling Time of Outputs

- **256Mb** NOR Falling Time(K8A5615ETA, K8A5615EBA)
(Test Condition : $V_{cc} = 1.7V$, Temp. = $85^{\circ}C$)



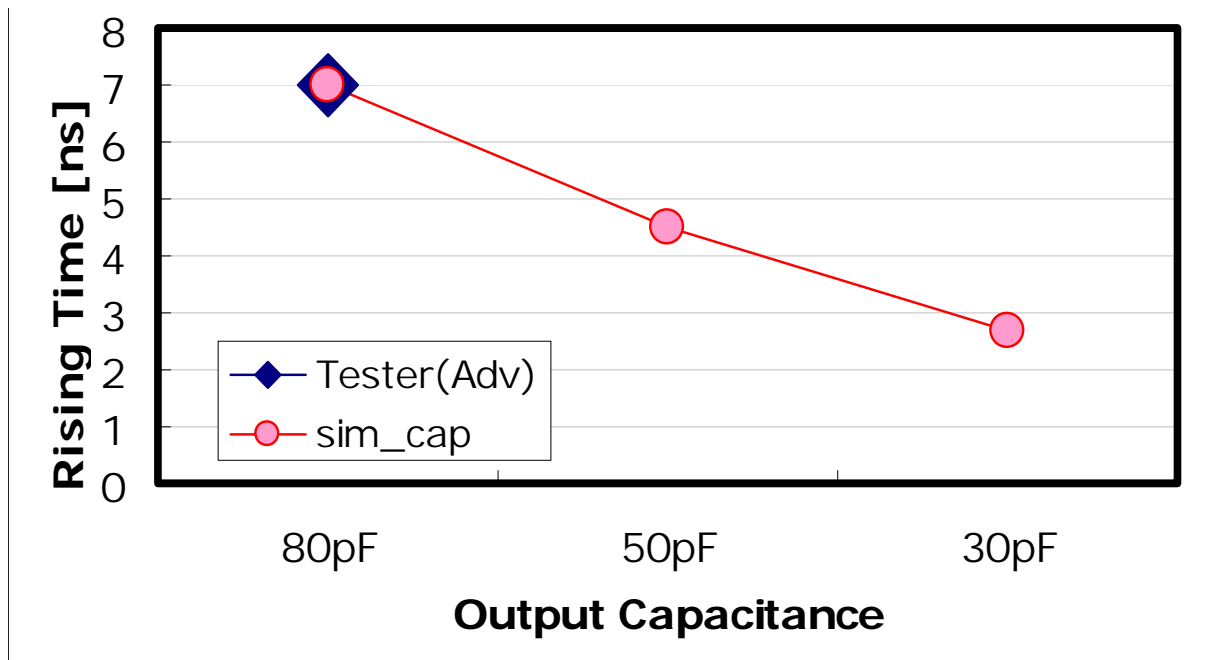
→ Because all of outputs have a same pad structure, the Simulation Value of falling slope have a same value.

Rising & Falling Time of Outputs

128Mb/64Mb NOR Rising Time

(K8A2815ETB, K8A2815EBB, K8A6415ETB, K8A6415EBB)

(Test Condition : $V_{cc} = 1.7V$, Temp. = 85°C)



Rising & Falling Time of Outputs

128Mb/64Mb NOR Falling Time

(K8A2815ETB, K8A2815EBB, K8A6415ETB, K8A6415EBB)

(Test Condition : $V_{cc} = 1.7V$, Temp. = 85°C)

