The effect of Pull Up Resistance and Load Capacitance to R/$\overline{B}$ pin's slope

SEP. 30th, 2005

Product Planning & Application Engineering Team

MEMORY DIVISION
SAMSUNG ELECTRONICS Co., LTD

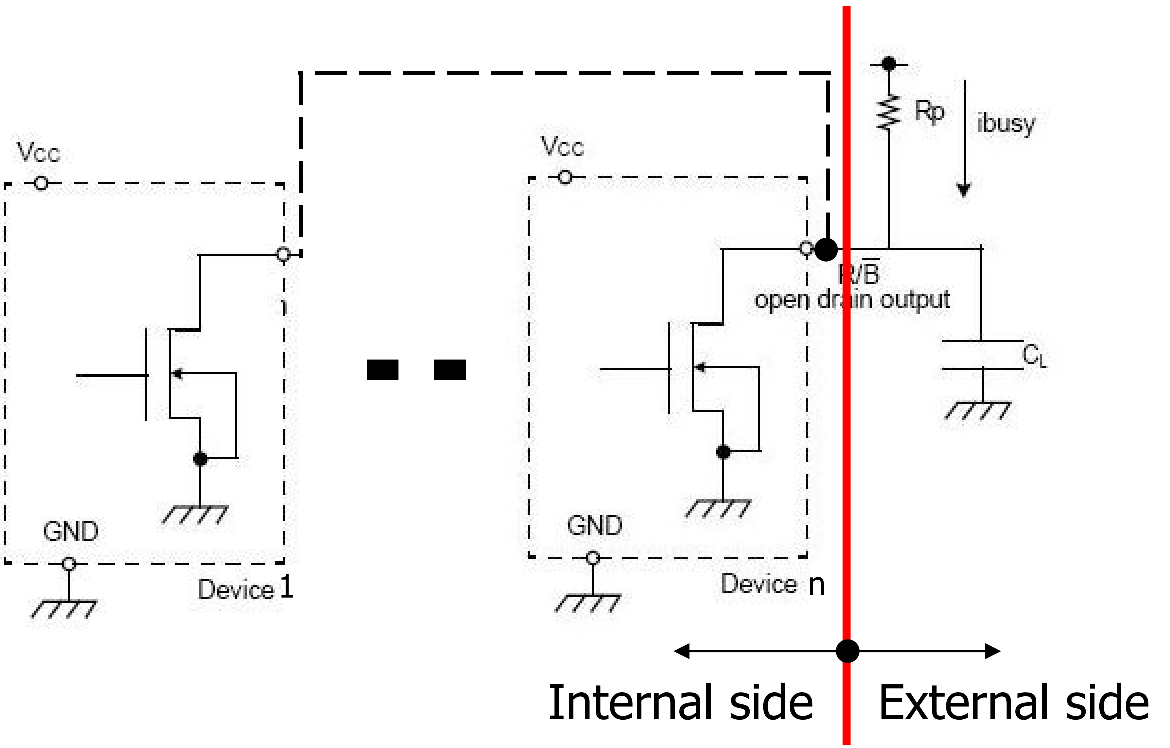
R/$\overline{B}$ pin's application

- Indicates the internal controller operation
  - Indicating the completion of a page program, erase, random read, and read (at 128KB block sized NAND) operation.

1. High state : Normal mode
   - Ready for operation
   - Completion of operation
2. Low state : Busy mode
   - After the program or erase or read command is written to the command register
   - Random read is started after address loading.

Circuit Diagram of R/$\overline{B}$ pin

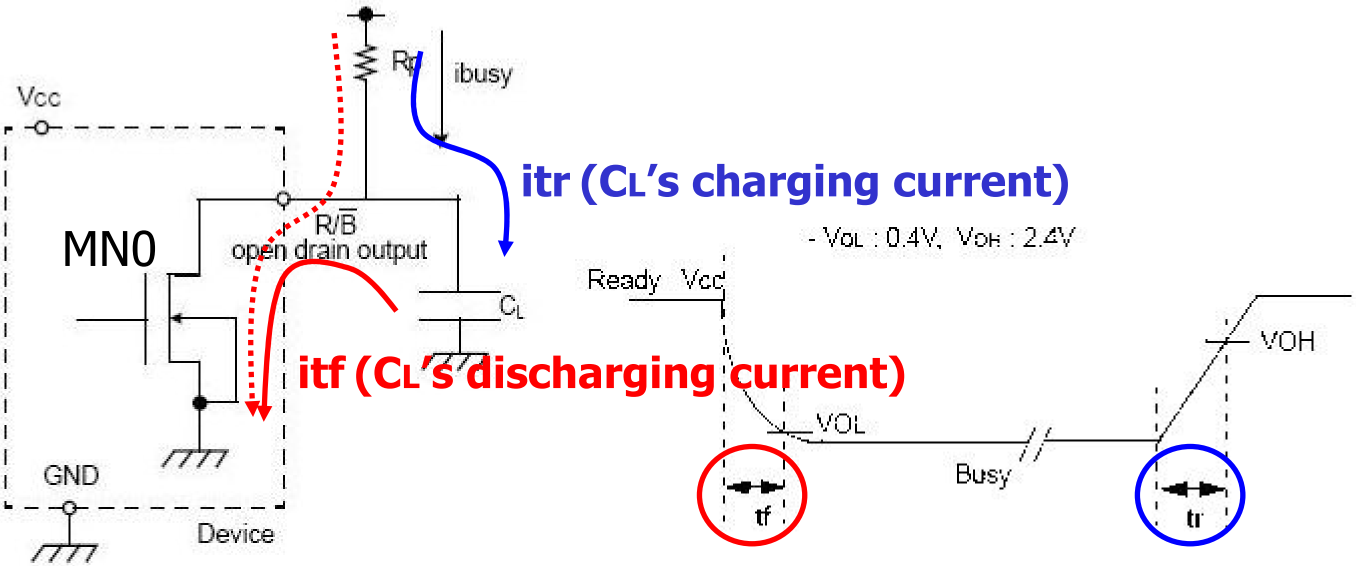
- Two or more R/$\overline{B}$ outputs to be OR-tied



- In case of Multi-chip package, more than one R/$\overline{B}$ would be connected.
- Or-Tied means if one or more of devices are busy state, then the output of R/$\overline{B}$ will be LOW state (busy state).

Relationship with Signal slope

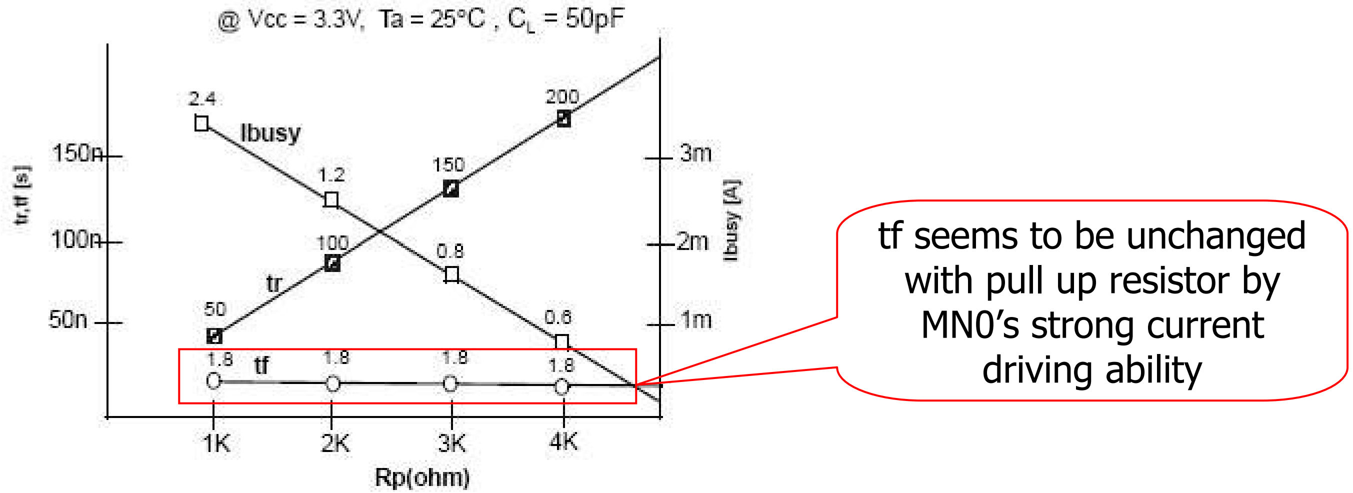
- Time of falling and rising are related to Rp, and C_L



- itf is controlled by MN0's current driving ability
  - The driving ability of MN0 transistor is assumed to be sufficient enough to drive tf as rapidly as expected
  - Ibusy electric current also affects the tf, but the level may be not so good to compare to Charged electric charge in the load capacitor C_L

Simple description about tr

- The relation of slope time, Rp, and Ibusy
  - Guided by specification of K9F2G08U0M



- i_{tr} is controlled by Rp's value (assumed that C_L is constant)
  - Δq (electric charge quantity variation) = i (electric current) * Δt (time variation)
  - V (voltage) = I (electric current) * R (resistance value)
  1. i_{tr} (electric current) may be inverse proportion relation to tr (charging time)
  2. I (electric current) is inverse proportion relation to R (resistance value)
- The relationship of tr with electric current, and pull up resistor from above figure
  - I1 * tr1 = I2 * tr2 = I3 * tr3 = I4 * tr4(changing Rp affects Ibusy)
    - 2.4mA * 50ns = 1.2mA * 100ns = 0.8mA * 150ns = 0.6mA * 200ns
  - tr1 $\propto$ Rp1, tr2 $\propto$ Rp2, tr3 $\propto$ Rp3, tr4 $\propto$ Rp4
    - 50ns $\propto$ 1K, 100ns $\propto$ 2K, 150ns $\propto$ 3K, 200ns $\propto$ 4K

Simple description about Ibusy

❑ The switch-on resistance (Ron) value of MN0 (at page 4)

- Its value is SMALL enough TO be IGNORED in comparison to Rp
- The resistance value of the path of Vcc to GND is Rp + Ron (expect 20Ω)
  - But, Ron << Rp means
    - Rp + Ron ≈ Rp
  - **So, the resistance value of the path of Vcc to GND is about Rp**

❑ By the Ohm's Law

- V_{OH} = Ibusy * Rp
  - Reference voltage is V_{OH} (2.4V)
- In case of Rp
  - Rp = 1KΩ/ 2KΩ/ 3KΩ/ 4KΩ
    - V_{OH}(2.4V) = Ibusy * Rp
    - Ibusy = 2.4mA/1.2mA/0.8mA/0.6mA

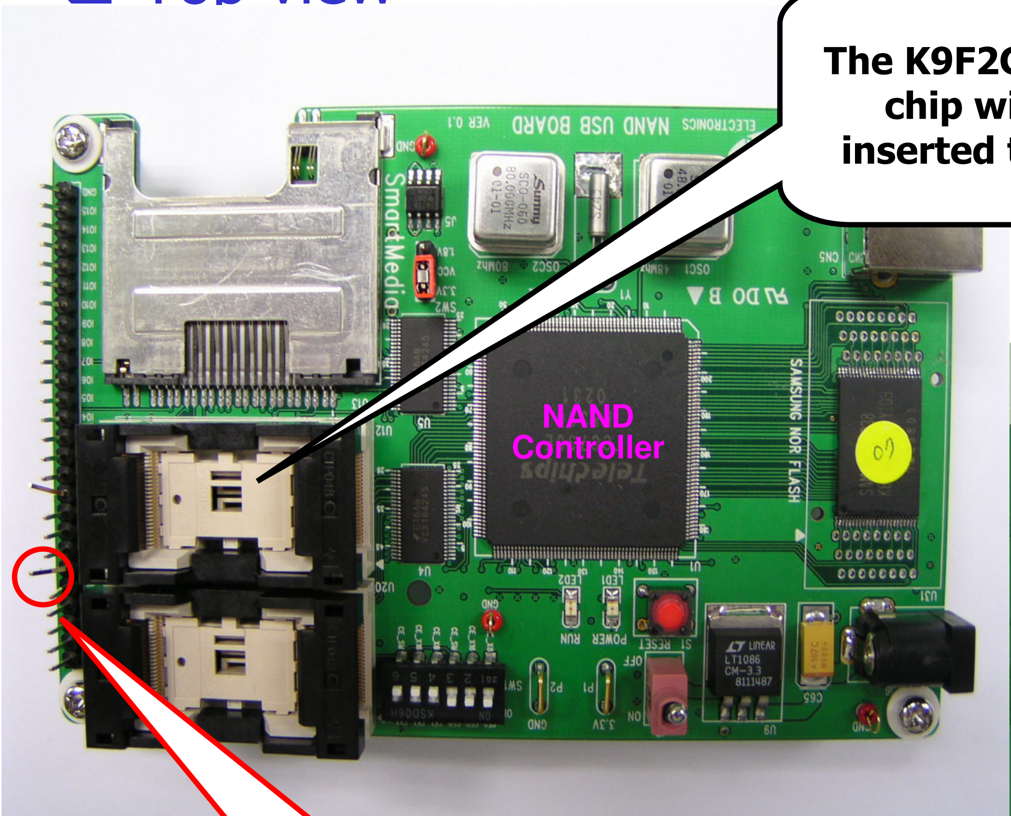
Simple expectation of C_L change

- V = I * R (Ohm's Law)
  - If Voltage V and resistance value R are not changed, then electric current I is not changed.
- Q = I * T (Preservation Law of Electric charge quantity)
  - Additionally, Q (electric charge quantity) = C (Capacitance) * V (Voltage)
  - The C value is directly proportional to the I value
    - Q = C * V = I * T
      - If V and I are not changed ,then C is directly proportional to T
  - Case of Rp = 1KΩ
    1. If C is decreased to 5 times (C_L = 10pF, referred to the figure of page 5), then tr will be decreased to 5 times (tr ≈ 10ns)
    2. If C is increased to 5 times (C_L = 250pF), then tr will be increased to 5 times (tr ≈ 250ns)

    ** The value of tr ≈ 250ns may be the same result of C_L=50pF, Rp = 5KΩ*
- $\tau = C * R$
  - The rising time is directly calculated by this equation

Test environment

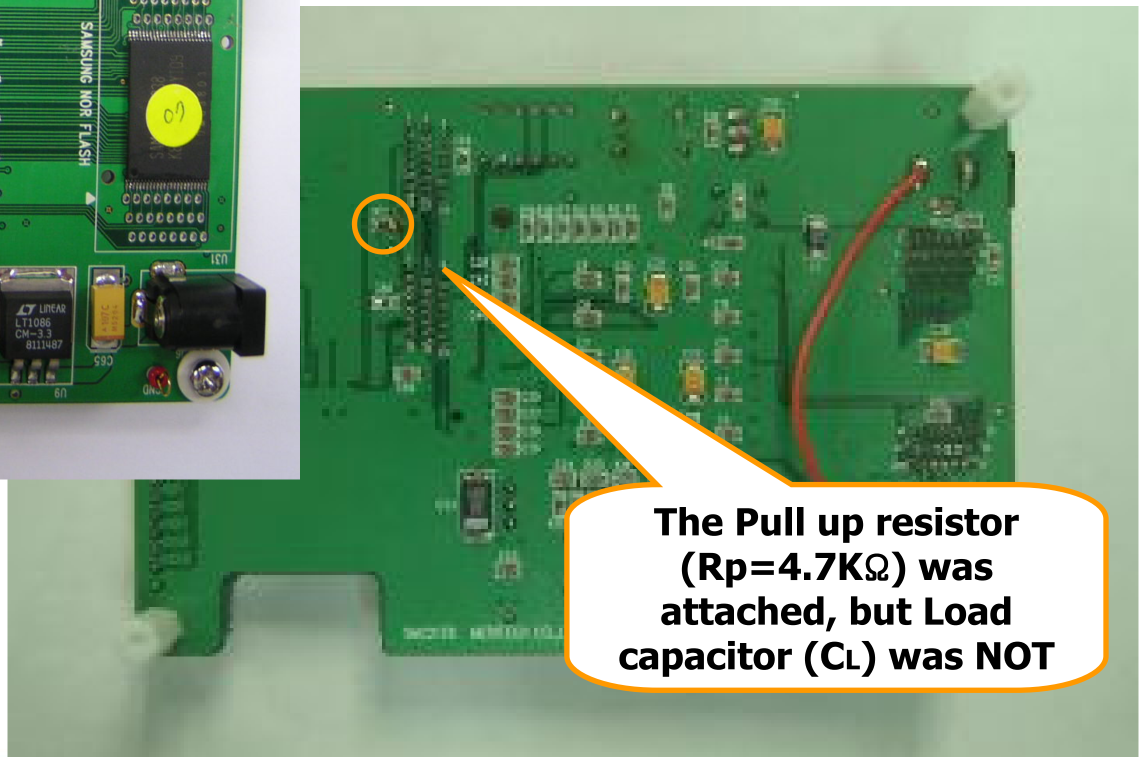
- Top view



The K9F2G08U0M chip will be inserted to here

The R/$\overline{B}$ signal will be measured by this test pin

- Bottom view



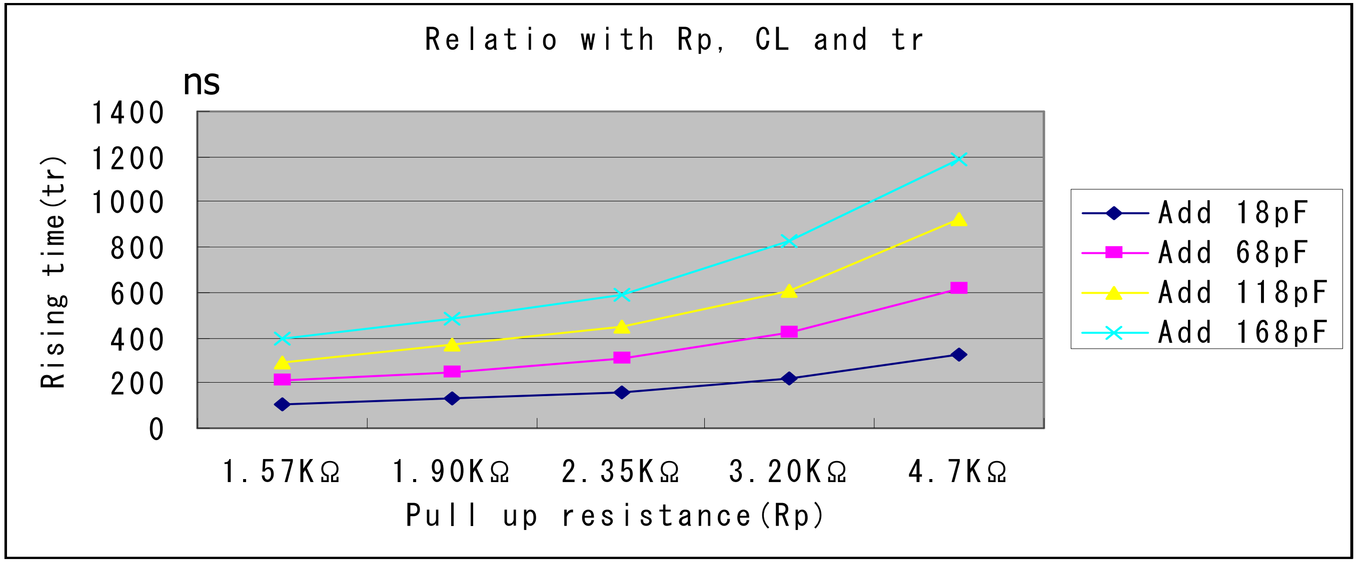
The Pull up resistor (R_p=4.7KΩ) was attached, but Load capacitor (C_L) was NOT

Test result of tf, tr with Rp, CL change

❑ Change of Rp, and CL (at K9F2G08U0M)

tf : Vcc to VOL(0.4V)
tr : GND to VOH(2.4V)

	Additional Load Cap.	Rp				
		1.57KΩ	1.90KΩ	2.35KΩ	3.20KΩ	4.7K
tf		1ns	1ns	1ns	1ns	1ns
tr1	18pF	104ns	128ns	162ns	218ns	322ns
tr2	68pF	207ns	244ns	310ns	420ns	616ns
tr3	118pF	294ns	374ns	452ns	604ns	928ns
tr4	168pF	392ns	484ns	588ns	832ns	1190ns



Test result analysis

Expect Initial Load Cap. by previous table

- By the tr1 with the condition of 4.7KΩ of pull up resistor
  - $tr_{4.7K\Omega}$ = (C_{Init} + 18pF) * 4.7KΩ = 322ns
  - C_{init} = 50pF

Measure initial load capacitance

- By HP4284A equipment
  - Which measures the initial load capacitance and initial resistance of node, etc
- The R/$\overline{B}$'s initial load capacitance is 67pF
  - This shows that the tr_{67pF} of 4.7KΩ's pull up resistor must have longer time than measured value(322ns)
    - 322ns : X = 50pF : 67pF
    - X = 399ns
  - At the tr2

	1.57K	1.9K	2.35K	3.2K	4.7K
Measured	207ns	244ns	310ns	420ns	616ns
Expected	201ns	243ns	300ns	409ns	601ns

The difference of expect and measure

- All of passive devices have the error rate (about 10%) even the measurement equipment
- May be the error rate of each device affects the difference including Human Error.
- But, at the tr2 the expected value and the measured value are nearly same.