

# **Bus Signal Line Load for The MultiMediaCard**

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**MEMORY DIVISION**

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# Bus Signal Line Load Issue

## ● Introduction

Even though Bus Signal Load was defined under NID spec, the most application manufacturers are violating total capacitance CL value by EMI & ESD stabilization purpose. By doing so, there are recognition failure with wrong command 1 response because of slowness of rising time slope in open-drain mode.

Therefore, Samsung recommend following guide line to manufacturers for preventing compatibility failure.

# RCMD & RDAT value guidance

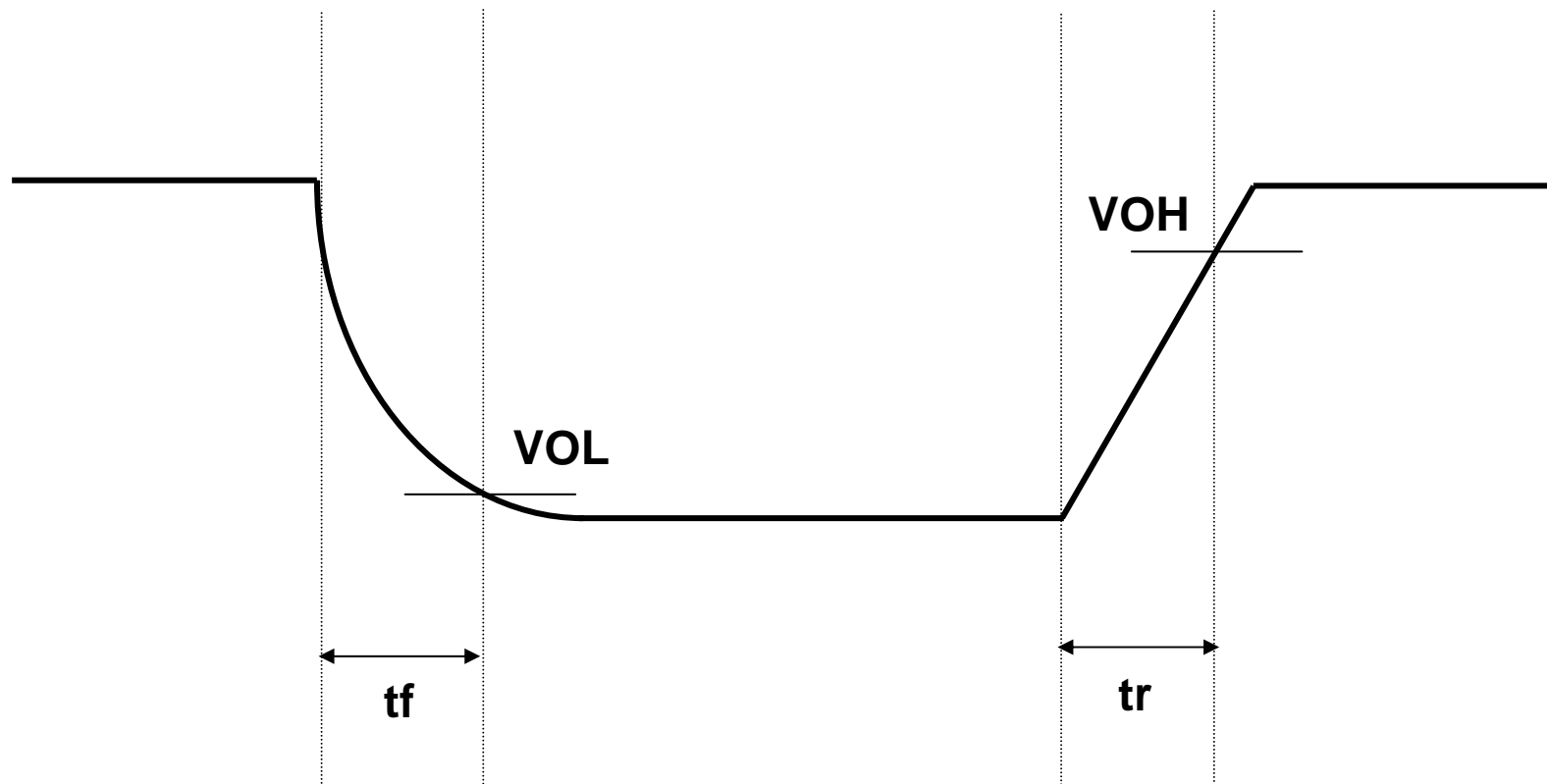
Parameter	Symbol	Unit	Specification		Recommend (SEC)	Note
			Min	Max		
Pull-up resistance for CMD	R <sub>CMD</sub>	KOhm	4.7	100	10	to prevent bus floating
Pull-up resistance for DAT0-7	R <sub>DAT</sub>	KOhm	50	100	-	to prevent bus floating
BUS signal line capacitance	C <sub>L</sub>	pF	-	20	-	Single card
Maximum signal line inductance		nH	-	16	-	fpp <=52MHz

☞  $C_L = C_{HOST} + C_{BUS} + C_{CARD}$

☞  $C_{HOST} + C_{BUS} = 20\text{pF}$  (High Speed Card) or  $30\text{pF}$  (Backward Compatible Card)

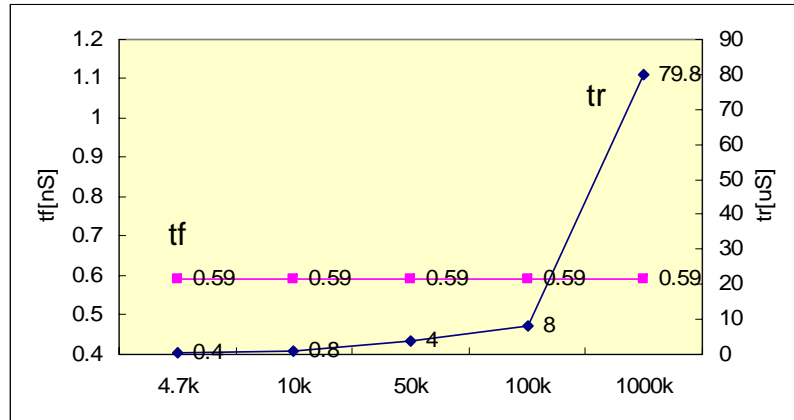
# Result of Simulation (1)

- High Voltage →  $VOH : 0.75 * VDD$ ,  $VOL : 0.125 * VDD$
- Dual Voltage →  $VOH : VDD - 0.2V$ ,  $VOL : 0.2V$



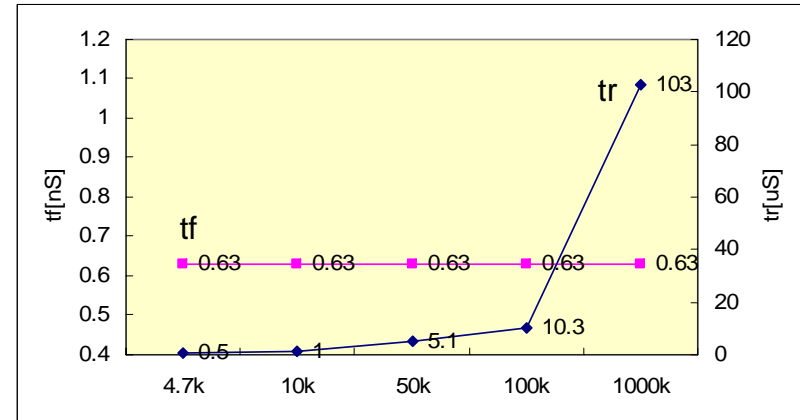
# Result of Simulation (2)

@ VDD = 3.3V, Ta=-25°C, CL=20pF



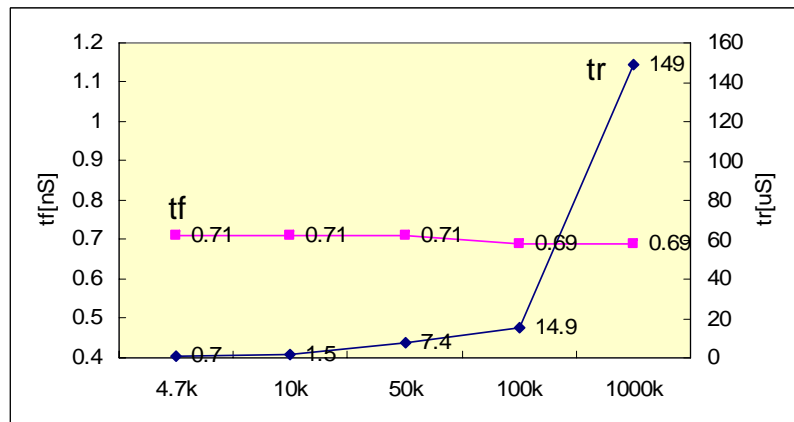
RCMD [ohm]

@ VDD = 3.3V, Ta=-25°C, CL=30pF



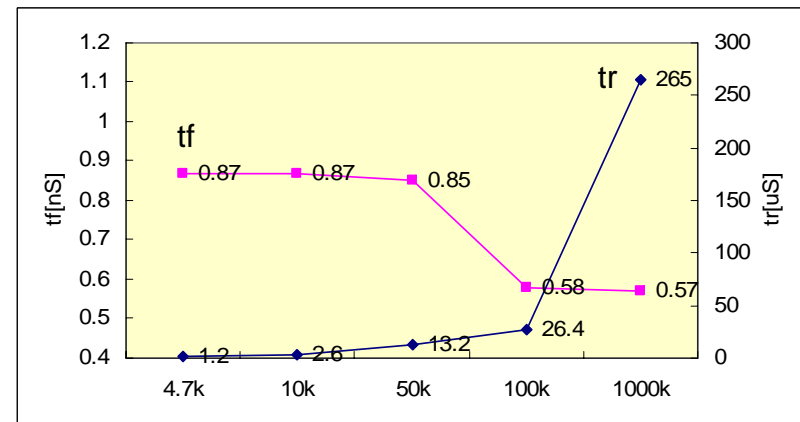
RCMD [ohm]

@ VDD = 3.3V, Ta=-25°C, CL=50pF



RCMD [ohm]

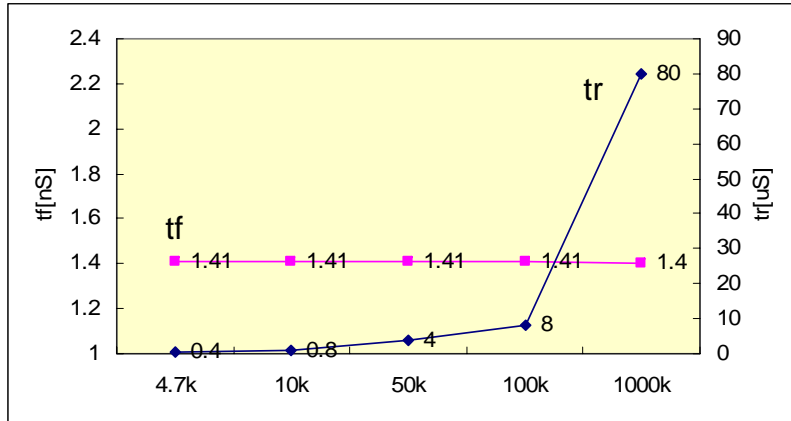
@ VDD = 3.3V, Ta=-25°C, CL=100pF



RCMD [ohm]

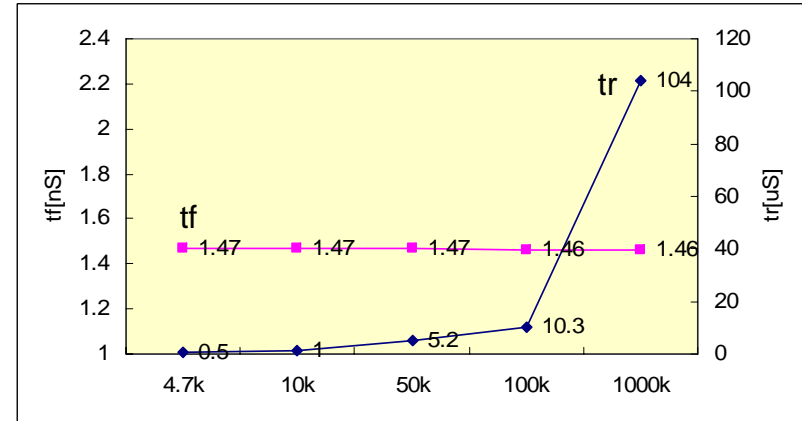
# Result of Simulation (3)

@ VDD = 1.8V, Ta=-25°C, CL=20pF



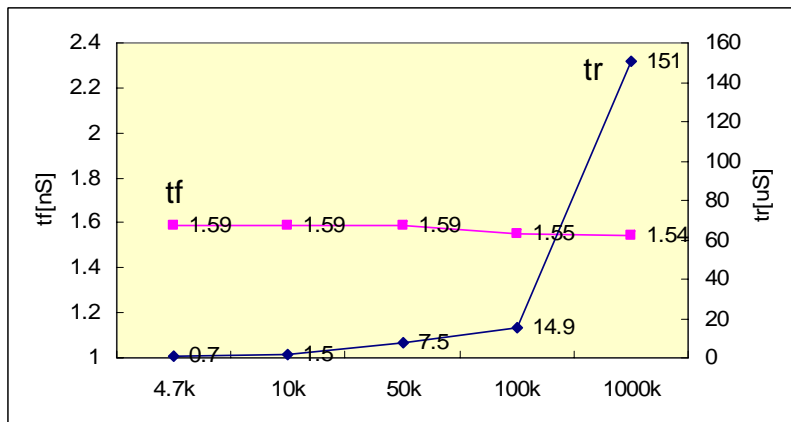
RCMD [ohm]

@ VDD = 1.8V, Ta=-25°C, CL=30pF



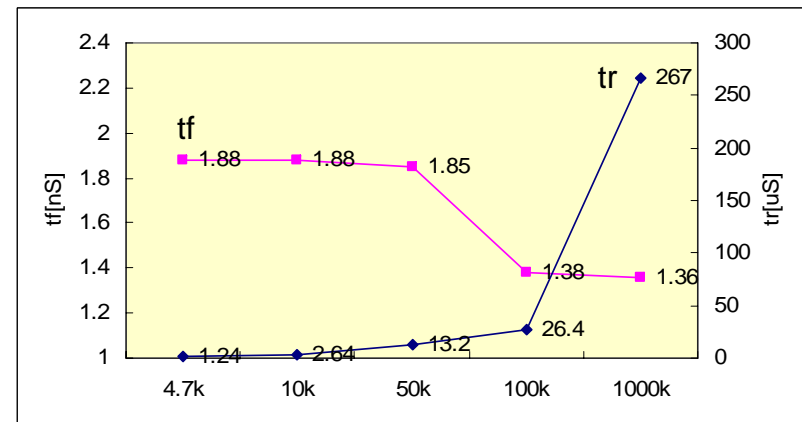
RCMD [ohm]

@ VDD = 1.8V, Ta=-25°C, CL=50pF



RCMD [ohm]

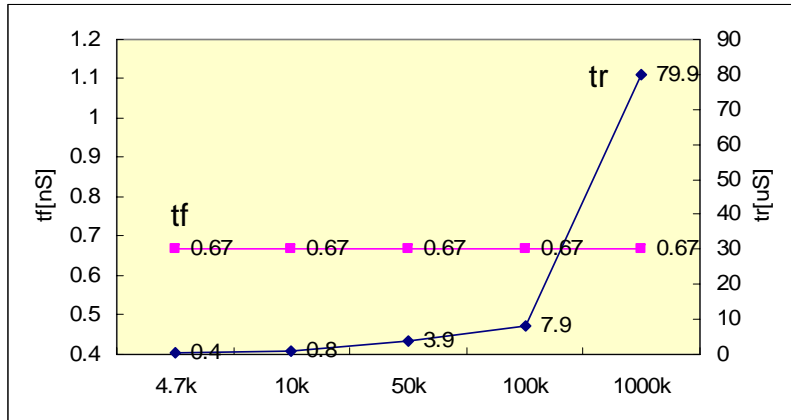
@ VDD = 1.8V, Ta=-25°C, CL=100pF



RCMD [ohm]

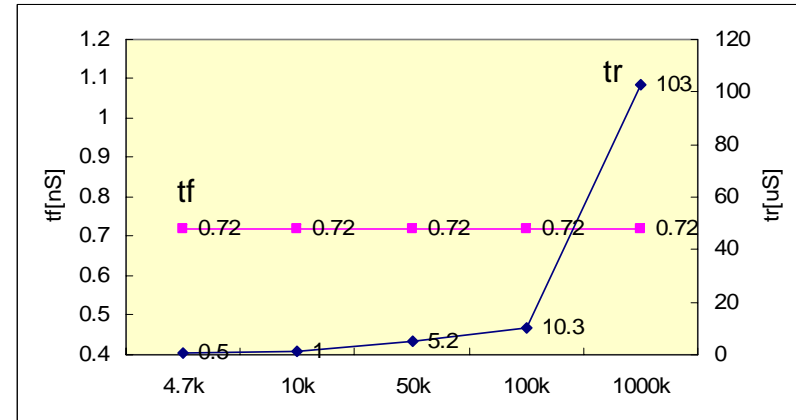
# Result of Simulation (4)

@ VDD = 3.3V, Ta=25°C, CL=20pF



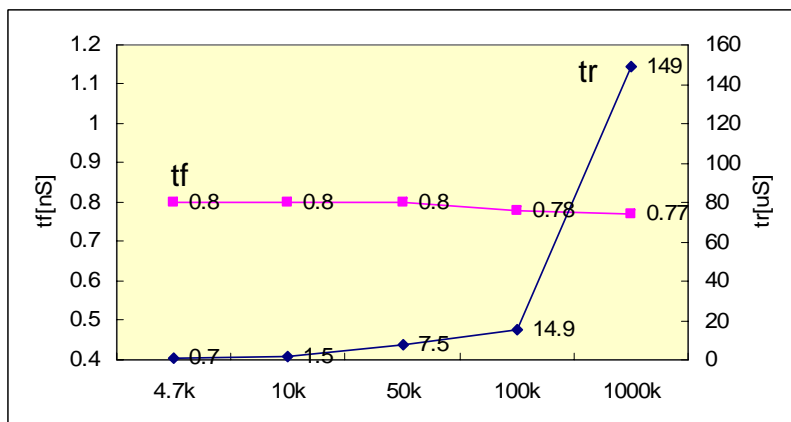
RCMD [ohm]

@ VDD = 3.3V, Ta=25°C, CL=30pF



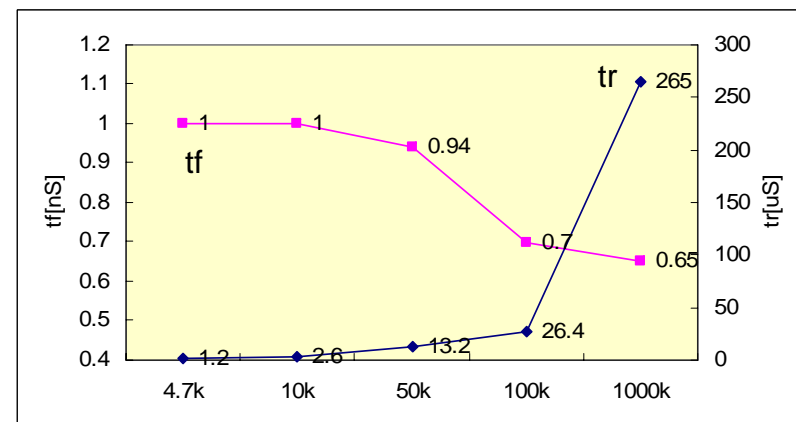
RCMD [ohm]

@ VDD = 3.3V, Ta=25°C, CL=50pF



RCMD [ohm]

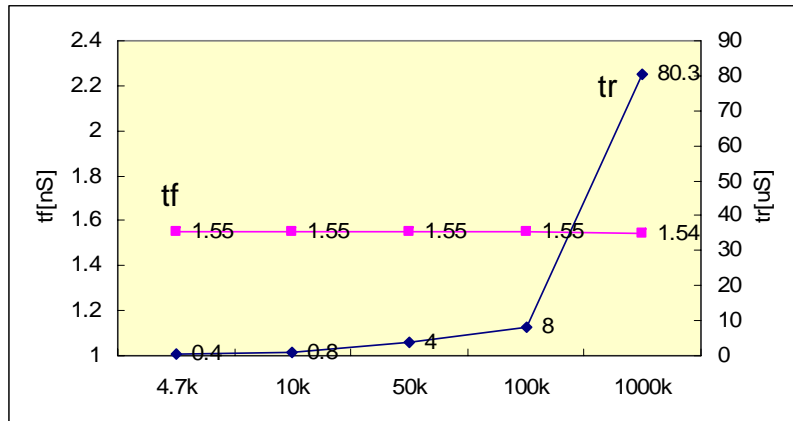
@ VDD = 3.3V, Ta=25°C, CL=100pF



RCMD [ohm]

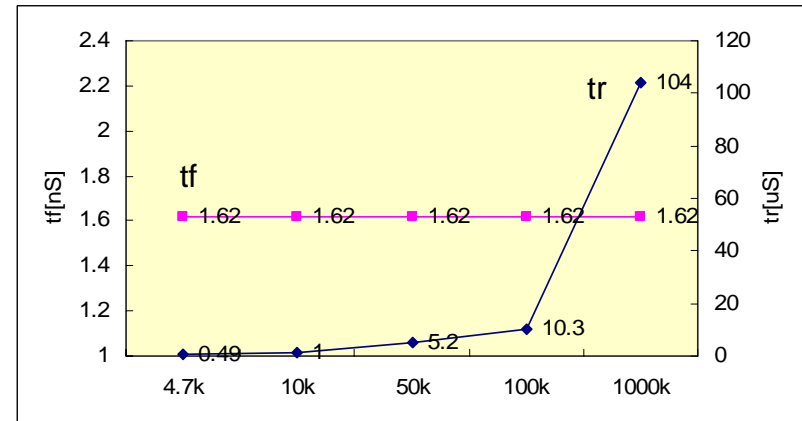
# Result of Simulation (5)

@ VDD = 1.8V, Ta=25°C, CL=20pF



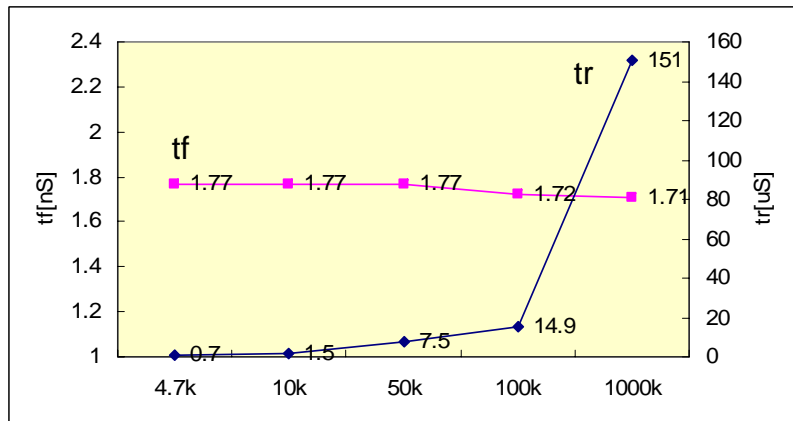
RCMD [ohm]

@ VDD = 1.8V, Ta=25°C, CL=30pF



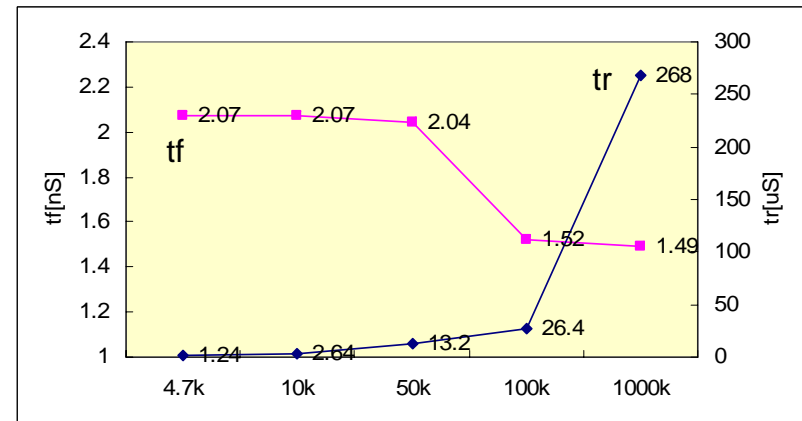
RCMD [ohm]

@ VDD = 1.8V, Ta=25°C, CL=50pF



RCMD [ohm]

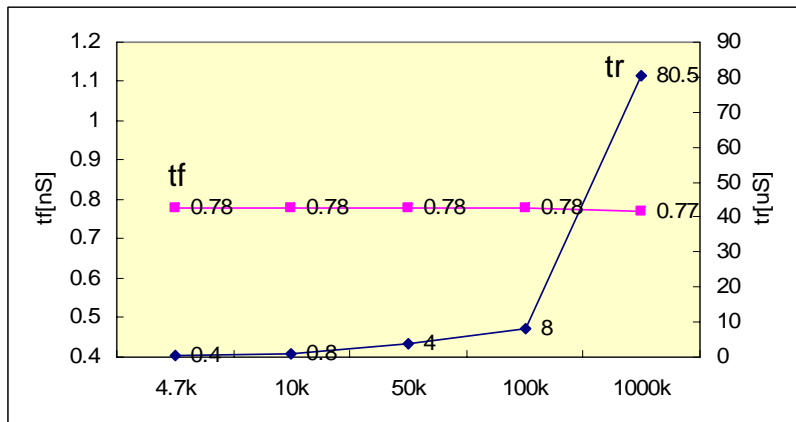
@ VDD = 1.8V, Ta=25°C, CL=100pF



RCMD [ohm]

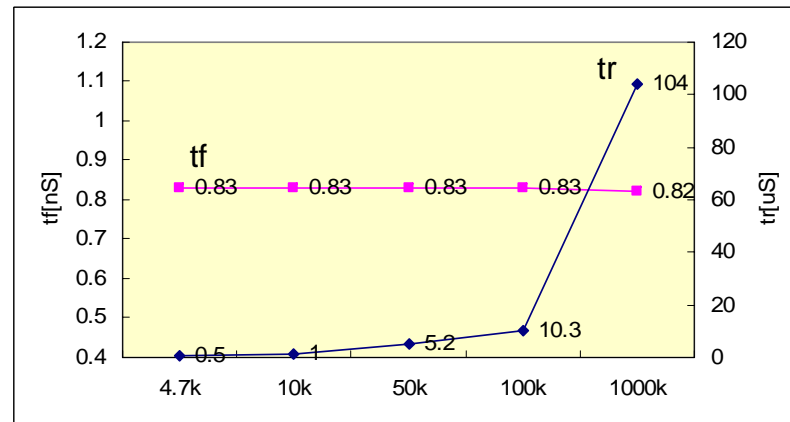
# Result of Simulation (6)

@ VDD = 3.3V, Ta=90°C, CL=20pF



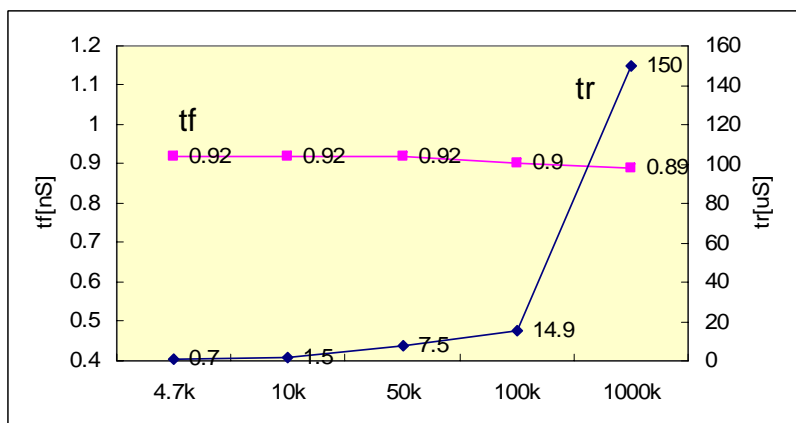
RCMD [ohm]

@ VDD = 3.3V, Ta=90°C, CL=30pF



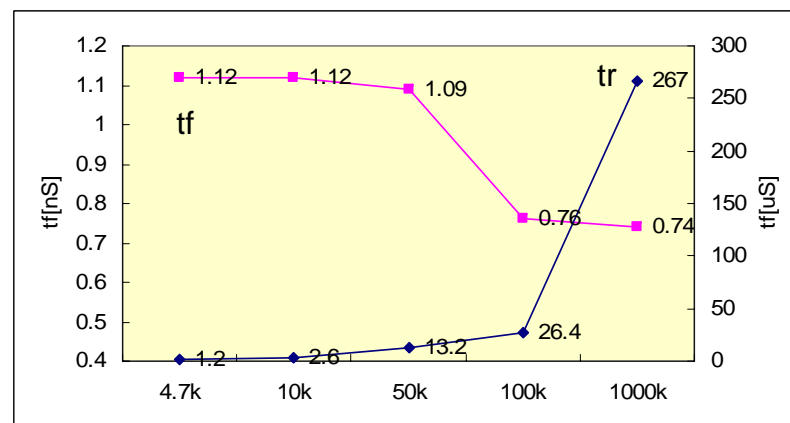
RCMD [ohm]

@ VDD = 3.3V, Ta=90°C, CL=50pF



RCMD [ohm]

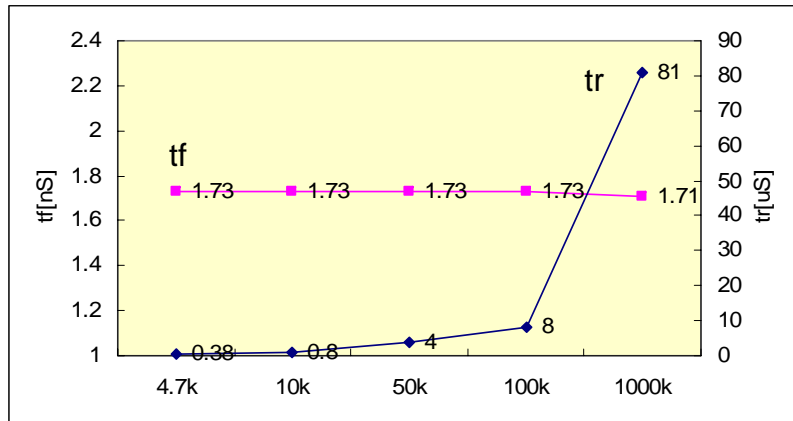
@ VDD = 3.3V, Ta=90°C, CL=100pF



RCMD [ohm]

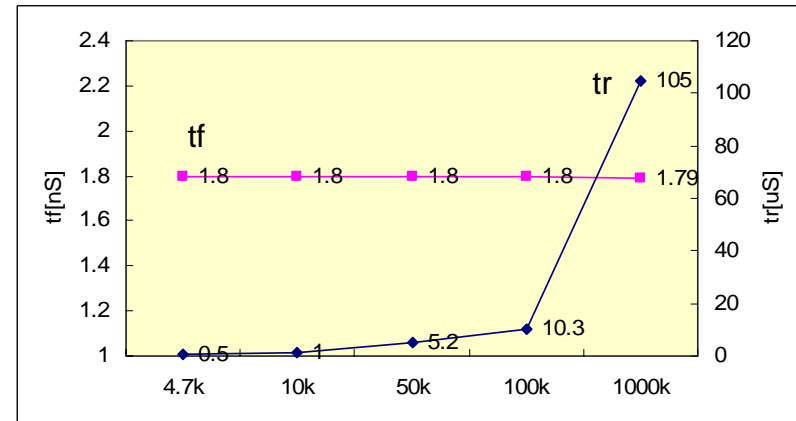
# Result of Simulation (7)

@ VDD = 1.8V, Ta=90°C, CL=20pF



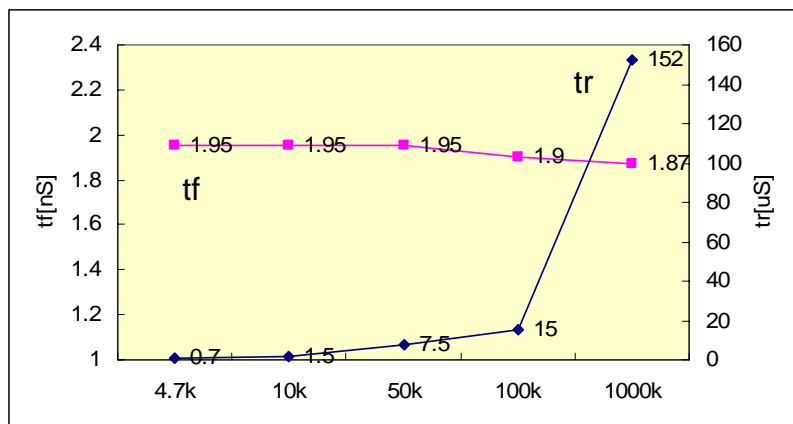
RCMD [ohm]

@ VDD = 1.8V, Ta=90°C, CL=30pF



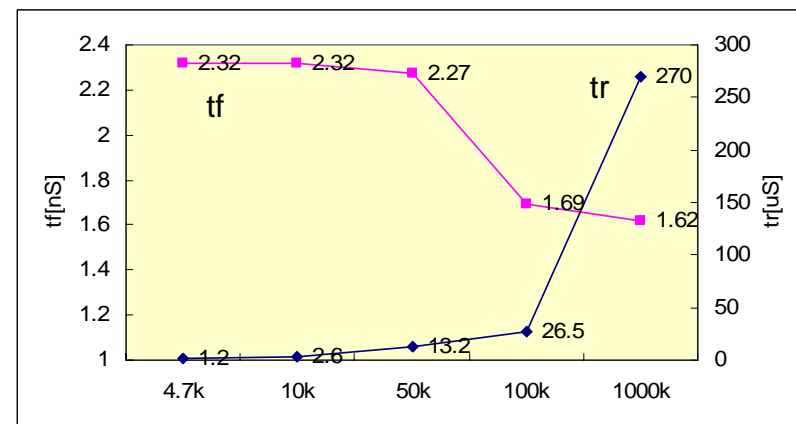
RCMD [ohm]

@ VDD = 1.8V, Ta=90°C, CL=50pF



RCMD [ohm]

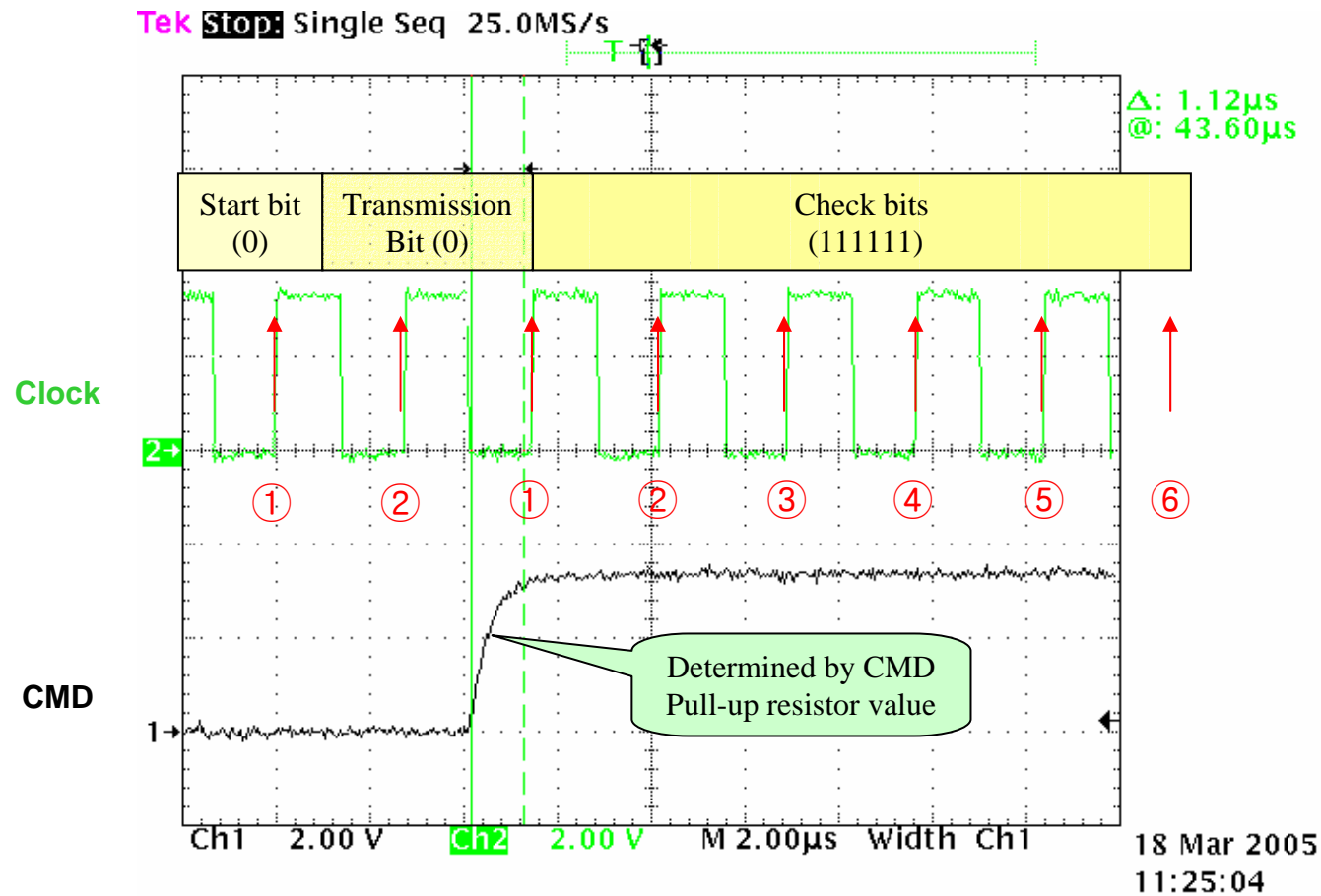
@ VDD = 1.8V, Ta=90°C, CL=100pF



RCMD [ohm]

# Signal Integrity (1)

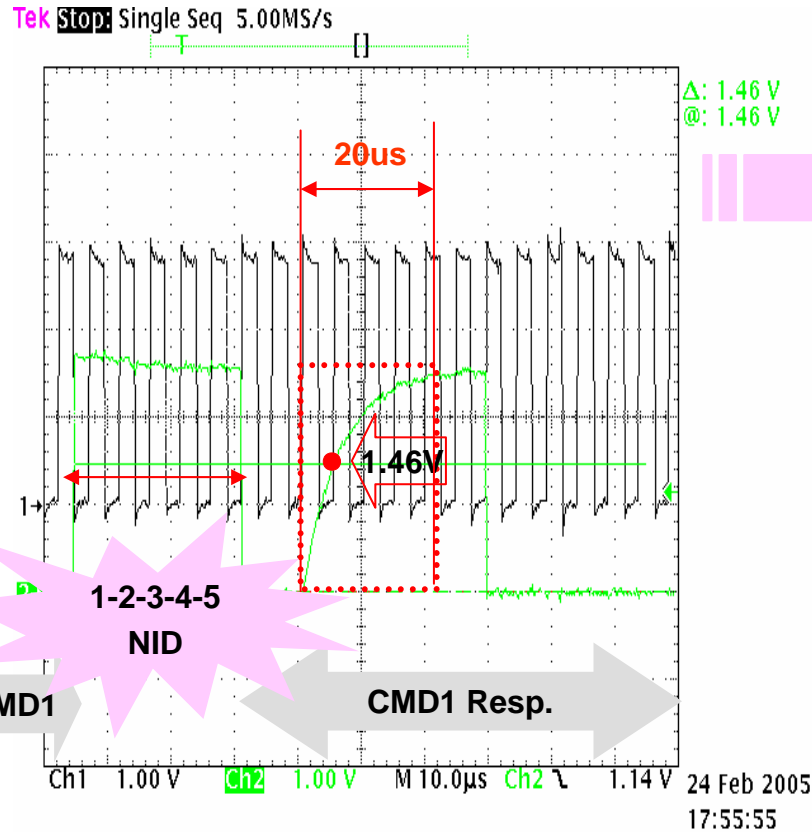
- R3 Response
  - ✓ CMD1 signal rise time in Card identification mode



# Signal Integrity (2)

- Host : Phone 2.7V, 200KHz (Card Identification mode)

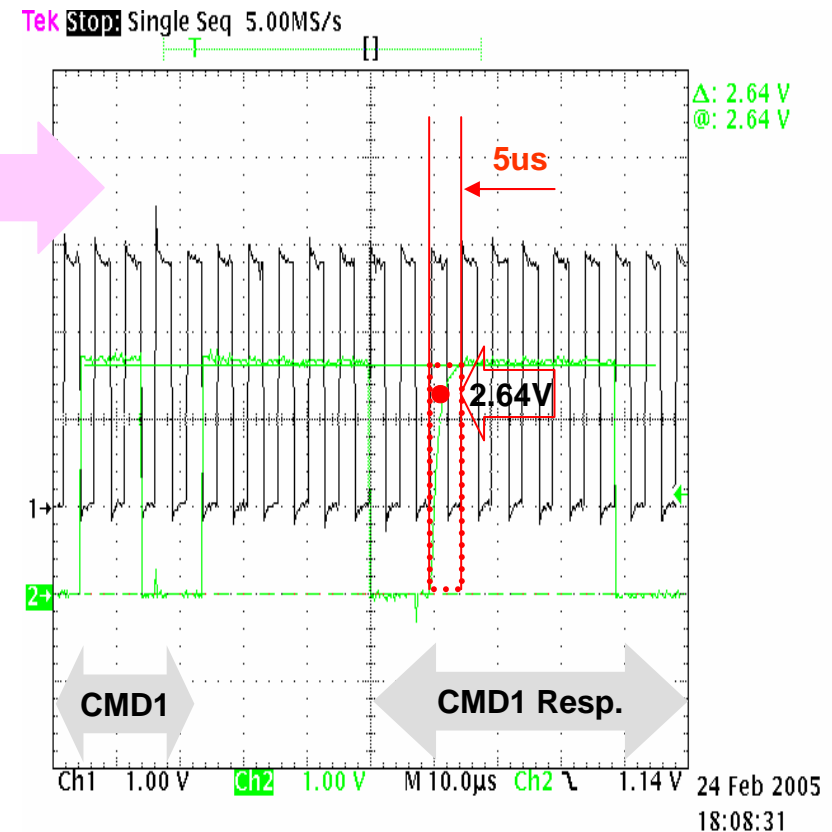
@ VDD = 2.7V, Ta=25°C, CL=67pF



RCMD=56K [ohm]

$C_{Host} (50pF) + C_{card} 17pF = 67pF$

@ VDD = 2.7V, Ta=25°C, CL=67pF



RCMD=10K [ohm]

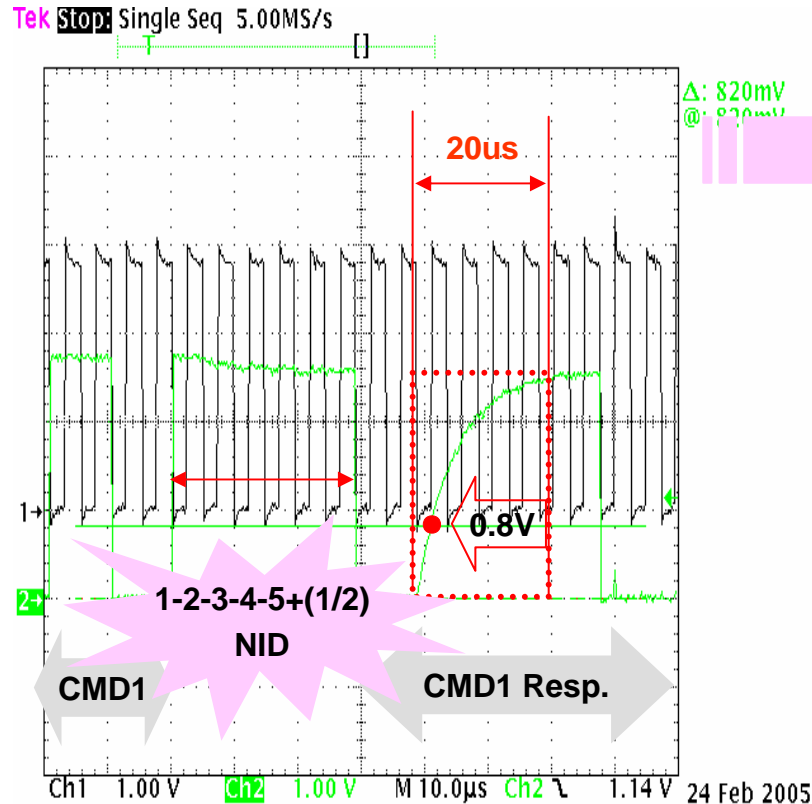
$C_{Host} (50pF) + C_{card} 17pF = 67pF$

# Signal Integrity (3)

The example of modifying pull-up resistor value, in case of NID spec. violation

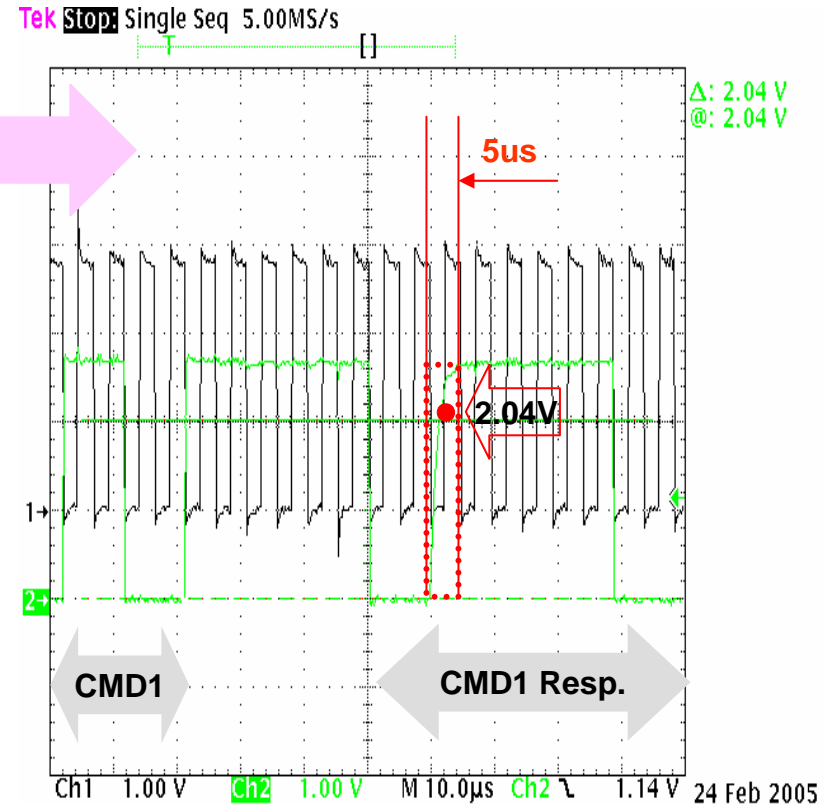
@ VDD = 2.7V, Ta=25 °C, CL=67pF

@ VDD = 2.7V, Ta=25 °C, CL=67pF



RCMD=56K [ohm]

$C_{\text{Host}} (50\text{pF}) + C_{\text{card}} 17\text{pF} = 67\text{pF}$



RCMD=10K [ohm]

$C_{\text{Host}} (50\text{pF}) + C_{\text{card}} 17\text{pF} = 67\text{pF}$