

# **XSR1.5 WEAR LEVELING**

## ***Application Note***

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## Introduction

A flash memory comprises a plurality of unit memory cells, each of which has one or more MOS transistors. Each transistor has two gates, a floating gate and a control gate. The floating gate is typically covered with an oxide film (SiO<sub>2</sub>), and the floating gate is located between a substrate and a control gate. The transistor can switch between two logic states by implanting or erasing electric charges into or from the floating gate. That is, when a relatively high voltage is applied to the control gate to generate a strong electric field between the control gate and substrate, electrons are moved from the substrate to the floating gate. If the voltage supply to the control gate is stopped, the electric charges on the floating gate do not escape from the floating gate to the external due to the oxide film, thereby storing data.

A limitation of Flash memory technology is that the number of times a unit can be erased is inherently limited by the physics of the Flash cell. Repeated erasure of a unit wears out the cells in the unit leading to a reduced capability to distinguish between the erased state and the programmed state, resulting in a longer time to erase the unit, appearance of sporadic faults in programming or erasing data, and ultimately the unit may lose entirely the ability to be erased and reprogrammed.

Since flash memory cells are degraded during the process of writing and erasing data, the memory cells must be checked to determine if a sector may be used before data is written to the sector. If the sector has degraded too much, the data is written to a different, less degraded sector. This process is called wear leveling.

The effects of wear are statistical in nature, and the ability of a Flash device to withstand wear is described by a number called the program/erase endurance. This number is the minimum or average number of times each Flash unit may be erased without encountering significant failures. Samsung ensures the endurance number to be at least 100K.

The limited endurance limits the lifetime of a Flash disk. It would be advantageous to have a lifetime that is as long as possible, and this depends on the pattern of access to the Flash disk. Repeated and frequent writes to a single unit, or a small number of units will bring the onset of failures soon and so end the useful lifetime of the media quickly. On the other hand, if writes can be evenly distributed to all

units of the media, each unit will experience close to the maximum number of erases it can endure, and so the onset of failures will be delayed as much as possible, maximizing the lifetime of the media.

## NAND Flash Architecture

NAND device is partitioned into fixed-sized blocks. The size of a block in a large block device is 128Kbytes. Each block is also partitioned into fixed sized pages. The page size of a large block is (2048 + 64) bytes. Each page is divided into an overhead area and a user's area. The user's area is a simple data storage area and the overhead area comprises a miscellaneous information area and an erasing tracking area for storing the number of times the sector has been erased. The miscellaneous information storage area stores various information regarding the sectors, including the physical address, valid bits and dirty bits. Each sector of the flash memory cell array must track data in an overhead area. Therefore, for any given capacity flash memory, the overhead area of the flash memory array increases the data storage requirements of the device. A significant portion of this additional data storage requirement is due to the portion of the overhead area used to track the number of times each sector has been erased. Due to errors that can occur during the manufacturing process, unit memory cells may fail to have uniform characteristics. For this reason, a particular memory cell may degrade more rapidly than other memory cells for the same number of data erasing operations. In this case, a part of a sector may be degraded, and fail to store data, even if the number of erasing times of the unit sector has not reached the reference number of erasing times obtained by testing. As a result, the data storing capacity of the whole sector is not reliable.

## Wear Leveling Technique

The algorithm of wear leveling in XSR is based on the simple idea. NAND flash memory can be erased on a block basis. With STL unit mapping algorithm, it can happen that the write command is concentrated in the specific block so that the specific block can be worn out quickly than most of the other blocks. To prevent this problem, STL keeps the erase count information of all units in each unit



header and considers the erase count when selecting a garbage unit. STL uses the unit with minimum erase count among all garbage units when the new unit is needed. Then STL can use units evenly without loss of efficiency. Garbage Queue is to manage garbage units and it sorts garbage units by the erase counts. XSR maintains two queues for garbage collection. All the dirty blocks that contain invalid sectors are put in to the garbage queue. When there is a need for new block, the blocks with the least erase count are erased and merged and put into the ready queue. When there is a need for a new block, the block with the least erase count from the ready queue is allocated for the write operation.

XSR also considers the boundary value parameter for performing the wear leveling. Difference between max erase count and min erase count is checked after unit write. The difference should be smaller than boundary. If difference is over boundary, STL makes min erase count unit into garbage unit (do merge operation). This is done to forcibly use less used unit by limiting the erase count difference between units within bound. Currently, boundary value is 1000 which is variable.

For 1 Gb OneNAND memory, each block can be erased and reprogrammed 100,000 times typically before the end of life. Even though the block reaches typical program/erase cycle, it is not marked as a bad block until there occurs an erase/ program failure.

### **Recommended Readings**

- Samsung XSR 1.5 Porting Guide, April 2006
- Samsung XSR 1.5 Pre-Programming Guide, April 2006
- Samsung NAND Flash Specification