
Board Guide for Noise Immunity



Title	Board guide for noise immunity.
Keywords	Board, noise
Abstract	This is a document about board guide for noise immunity.

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Revision History

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Board Guide Recommendations for Noise

1. Add 0.1uF/10uF bypass capacitor nearby the VDD pin, add more capacitors on the path of VDD. The 0.1uF is used to bypass high frequency noise and 10uF is to keep power source stable.

1.1 Decoupling capacitor

During active device switching, the high frequency switching noises spread to the power supply lines. The main effect of the decoupling capacitor is to provide a local source of DC power for the active devices, or current-needed IC. This reduces the high frequency noises propagating across the board.

Decoupling capacitor has to be placed close to MCU VDD-VSS pins below several mm distance, as shown in Fig.1, because trace between VDD-VSS pin and capacitor may act like inductance to intervene current flow.

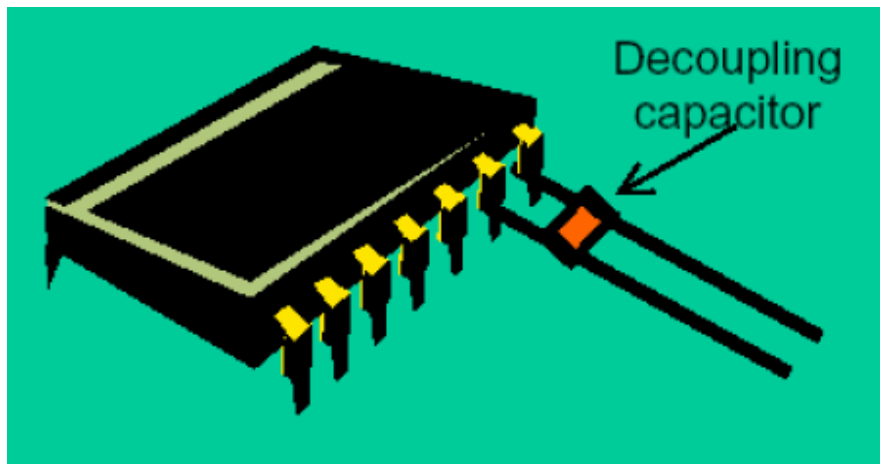


Fig.1 Position of a decoupling capacitor as close to MCU pin as possible

In case of placing a decoupling capacitor between VDD-VSS by using a via, the shorter trace length from via to pad is necessary so that the capacitor more effectively acts to reduce trace inductance.

The capacitance has to be evaluated during EMC tests. Start value could be 1nF or 100nF.

1.2 Bypass capacitor

This capacitor provides medium frequency current to the device as it forms the pulsed device current into average DC-current. Its main task is to keep the power supply stable. One or more bypass capacitor shall be connected to the local VDD.

The minimum capacitive value of the bypass capacitor required for optimal performance is determined by the maximum allowable amount of voltage drop across the capacitor as a result of a transient current surge. The require capacitance shall be calculated according to below formula.

$$C = \frac{I \Delta t}{\Delta U_o} \quad (\text{Equ.1})$$

with I = maximum average current for the supply-system

with Δt = operating clock period

with ΔU_0 = allowable voltage drop, default is 1%

Example:

For a 5.0V supply system the allowable voltage drop is $\Delta U_0 = 50\text{mV}$. With a 8MHz external oscillator the operating clock period is 125ns (non-divided CPU clock). If the average current consumption in the supply system to be decoupled is $I = 100\text{mA}$, the bypass capacitor should be $100\text{mA} \times 125\text{ns} / 50\text{mV} = 250\text{nF}$ (0.25 μF).

PCB layout:

Below figures show the incorrect PCB layout and correct ones.

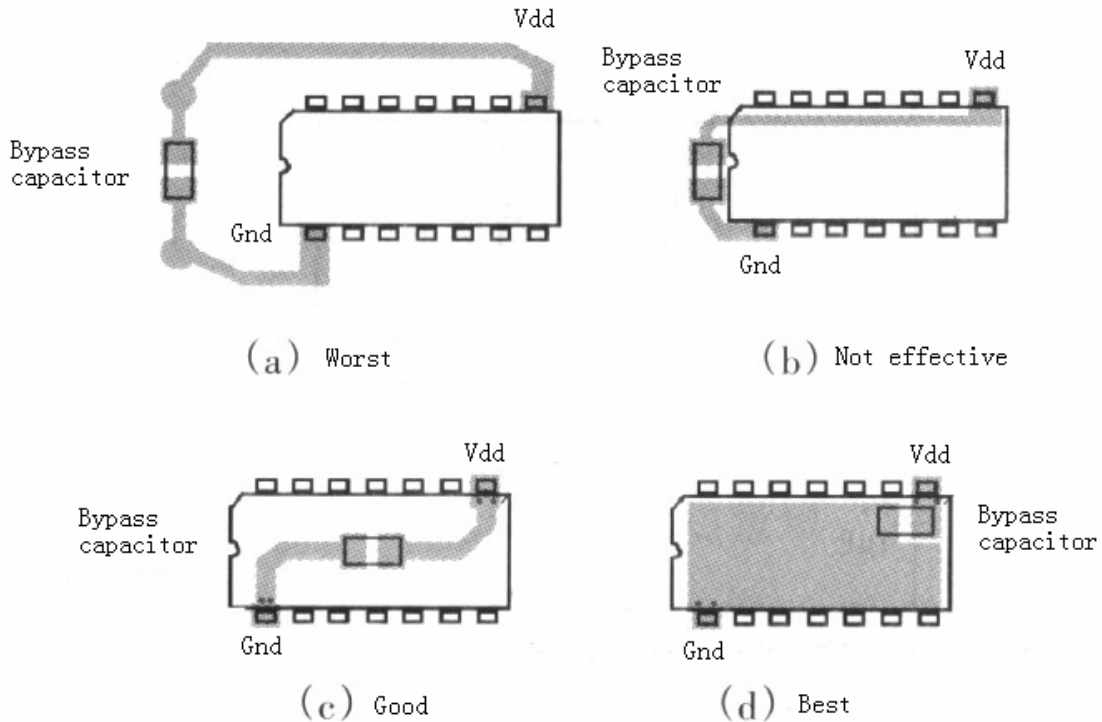


Fig.2 Position of a bypass capacitor as close to MCU pin as possible

Fig.2(a) shows an example of false placement. The capacitor is placed too far away from MCU pins, creating a large high current loop from VDD to VSS. As a result, noise is spread more easily to other devices on the board, and radiated emission from the board is increased even further, the whole high current loop will act as an antenna for the noise. Fig.2(b) is also not effective, Fig.2(c) is good for common application, and Fig.2(d) is the best.

In order to reduce the voltage ripple caused by ESR(Equivalent Series resistor) and ESL(Effective Series inductance), several capacitors in parallel may be required.

An ideal capacitor enables to pass the AC signal and to block the DC signal, but over specific frequency ranges, that is to say "self-resonance", the capacitor begin to block AC signal also. The characteristic of a capacitor changes in the higher frequency range, owing to lead inductance. Fig.3 shows equivalent circuit model of capacitor in a low and high frequency region. It suggests that capacitor behaves differently, depending on operating frequency region.

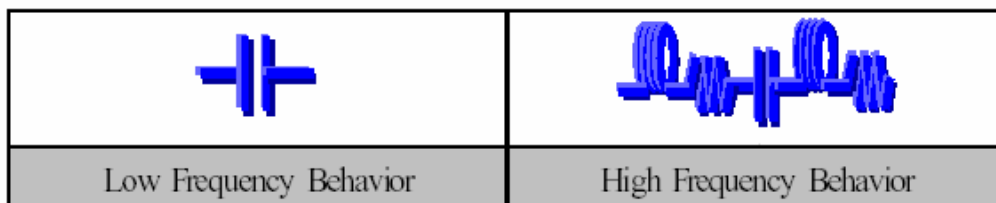


Fig.3 Equivalent circuit model of capacitor in a low and high frequency region

As we know, a capacitor has equivalent series resistor (ESR) and effective series inductance (ESL). In high frequency mode, the voltage ripple on VDD (ΔU_o) which make MCU work unstable can be described as below formula.

$$\Delta U_o = R_C \Delta i_C + \frac{1}{C} \int \Delta i_C dt + L_C \frac{d\Delta i_C}{dt} \quad (\text{Equ.2})$$

with R_C = equivalent series resistor (ESR) of bypass capacitor

with L_C = effective series inductance (ESL) of bypass capacitor

with Δi_C = current ripple

with C = capacitance of bypass capacitor

and its impedance absolute value can be described as

$$|Z| = \sqrt{R_C^2 + \left(\omega L_C - \frac{1}{\omega C}\right)^2} \quad (\text{Equ.3})$$

with $\omega = 2\pi f$, angular frequency

so, the self-resonant frequency depends on the equivalent series inductance and capacitance and it is approximately given by a following equation.

$$f = \frac{1}{2\pi\sqrt{L_C C}} \quad (\text{Equ.4})$$

where, f is resonant frequency.

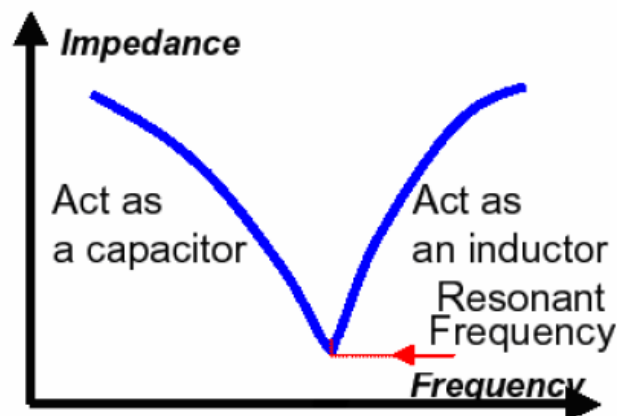


Fig.4 Impedance transition of capacitor

Fig.4 shows the impedance curve of capacitor versus frequency. As shown, with increasing frequency, the impedance decreases below the resonant frequency then increases. In other words, the capacitor is capacitive before the self-resonant but inductive after this. This characteristic change is due to the lead length and trace inductance. For filtering high frequency noise, high resonant frequency is required, so lower ESL is required according to Equ.4.

From Equ.1 and Equ.2, we also know that when capacitance is fixed, low ESR and low ESL is crucial to reduce voltage ripple. However, these capacitors with low ESR and ESL are expensive. So it's a good way to connect several capacitors in parallel. After that, ESR and ESL is reduced while capacitance the same. It makes voltage ripple lower and resonant frequency higher.

Example:

Three 0.1uF capacitors are connected in parallel to replace a 0.3uF capacitor.

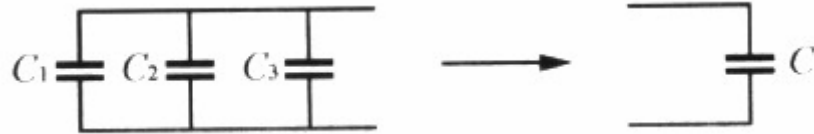


Fig.5 Connect several capacitors in parallel

2. Crystal/Ceramic must be close to MCU, the wire between them should be as short as possible. The capacitor for resonator must be placed between Crystal/Ceramic and MCU, the wire from capacitor to MCU should be as short as possible.

Oscillators are quite delicate devices and are, therefore, sensitive to external noise. Keep the oscillator loop as tight as possible. Place the crystal as close to the pins as possible. Connect the resonator capacitors directly to the MCU VSS pin.

Below figures show the incorrect PCB layout and correct ones.

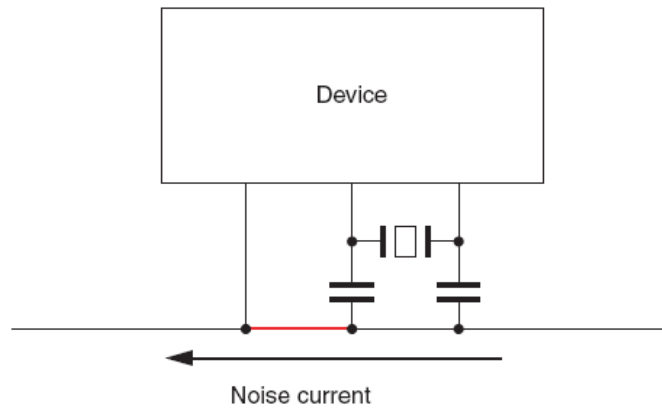


Fig.6 Poor oscillator ground

Although the impedance of a ground plane (loop) is low it is of course not zero. Therefore any noise current in the ground plane causes a voltage drop in the ground. If the 2 capacitors of the oscillator are connected directly to the ground plane (loop), the voltage drop in the red portion of the ground in Fig.6 will be overlaid to the oscillator signals. If the noise related voltage drop is big enough the oscillator may be disturbed.

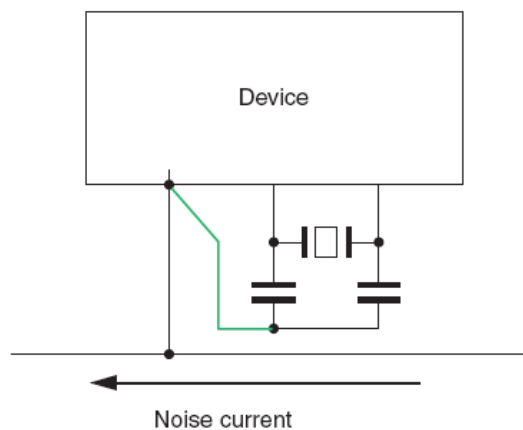


Fig.7 Optimal oscillator ground

The overlay of ground noise may be avoided by providing an extra ground trace for the oscillator ground as indicated in green in Fig.7. It is the best way to connect oscillator ground directly to MCU VSS pin.

3. Reset circuit must be close to MCU; reset capacitor must be the closest to MCU.

The most sensitive input signals in a MCU-based system, after the oscillator inputs, are the reset and interrupt input. These signals are easily corrupted by electromagnetic interference.

Below figures show the typical transient protection on reset and interrupt input pins.

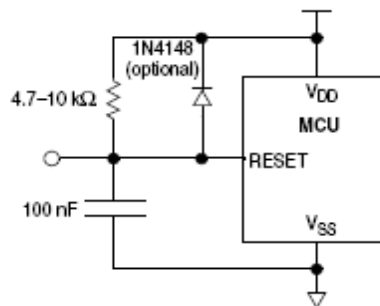


Fig.8 Typical transient Protection on Reset and Interrupt Input Pins

Place the reset circuit as close to MCU as possible. The VDD and VSS of reset must also be connected as close as possible to the VDD and VSS pins of MCU.

4. Unused pins should be configured as output pins or input pins. Unused input pins must be pulled down/up to VSS/VDD.

Transients on input signals create a particularly challenging problem. External noise could disturb MCU function through input pins. The standard protection for inputs is the low-pass filter as shown in Fig.9. The series resistor limits the injected current. The parallel capacitor shunts the transient current into the ground system as it attempts hold the voltage to its steady-state value.

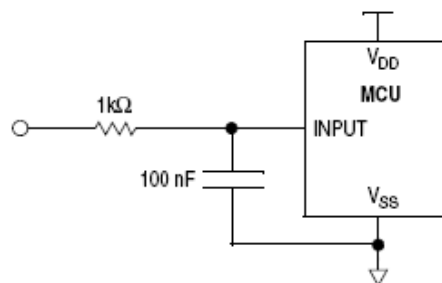


Fig.9 Typical Low-Pass Filter Transient Protection on Input Pins

Unused pins should be configured as output pins or input pins and connected to VSS/VDD.

5. Make large ground area. Or make ground loop and make sure the loop is the tightest. Drill in the ground area to make VSS signal has equivalent voltage.

All kinds of currents, AC or DC, high-power or low-power, signal or noise, are always trying to find the easiest path to ground. The basic idea behind many EMC design techniques is to control the path to ground for all signals, and make sure that this path is away from signals and circuits that may be disturbed.

The path to ground will always be the path of least impedance, and for a high-frequency signal, this is the path with the smallest loop, not the path that has lowest DC resistance. So if possible, one of the layers should be used as a dedicated ground plane and only that. But sometimes it is not applicable. Another way of designing a similar ground plane is to fill all unused space of the board and connect the ground planes together with vias wherever needed. It is very important to make sure that the ground plane at every part of the board covers at least one layer and that enough vias are used so that the total ground area becomes as complete as possible.

6. Follow the 3W Principle, the line spacing should be at least 3 times of the width. Xin/Xout pin should be surrounded by ground, to decrease EMI.

Both trace separation and guard trace are used to minimize the cross-talk and noise coupling by reducing magnetic flux coupling between adjacent on the PCB layer.

Fig.10 shows the schematic diagram of (a) 3W rule and (b) high speed clock between the guide traces. In Fig.10 (a), the 3W rule illustrates that the space between the traces should be greater than 2W. Note that the width of a trace is W. To further decrease magnetic coupling, the guard trace near critical signals such as high speed clock need to be isolated from other noises being coupled onto the signal lines. In Fig.10 (b), the high speed clock is between the guard traces connected to the ground through the vias. The magnetic flux will be captured from both the adjacent guard traces and vias. Thus, the distance from high speed clock trace to the guard traces should be as close as possible.

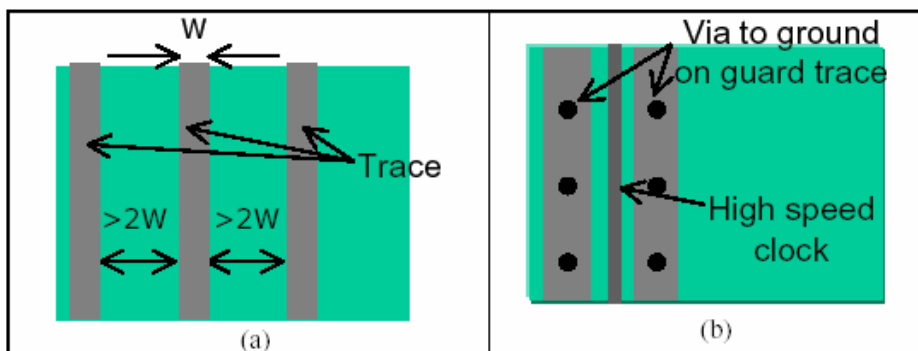


Fig.10 Schematic diagram of (a) 3W rule and (b) high speed clock between the guard traces
 Example: The adjacent ground pin implements a special guard ring around the oscillator circuit.

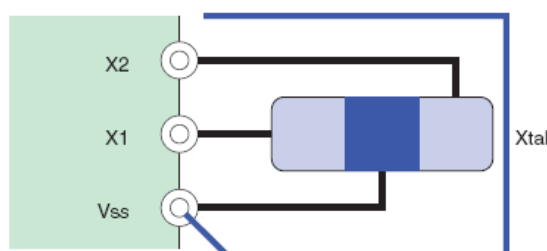


Fig.11 A Special Guard Ring Around the Oscillator Circuit

7. When normal operating, TEST pin had better be connected to VSS.

When high voltage (>VIH) is applied on TEST pin, MCU might enter Factory Test mode and work on an unknown status. Therefore, It's recommended that TEST pin be connected to VSS during normal operating.