

DDR Code Information(1/2)

Last Updated : November 2008

K **7** **D** X X X X X X X - X X X X X X X
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

1. Memory (K)

2. Sync(DDR) SRAM : 7

3. Small Classification

D : Double Data Rate

4~5. Density

40 : 4M 80 : 8M
16 : 16M 32 : 32M

6~7. Organization

18 : x18 36 : x36

8~9. Vcc, Interface, Mode

71 : 2.5V, HSTL, 3-1-1-1
74 : 1.8V/ 2.5V, HSTL, All

10. Generation

M : 1st Generation
A : 2nd Generation
B : 3rd Generation
C : 4th Generation

11. "—"

12. Package

H : BGA, FCBGA, PBGA
G : BGA, FCBGA, PBGA (Lead-Free)

13. Temp, Power

- COMMON (Temp, Power)

C : Commercial, Normal
I : Industrial, Normal

14~15. Speed

- Other Small Classification (Clock Cycle Time)

33 : 333MHz 35 : 350MHz
37 : 375MHz 40 : 400MHz

DDR Code Information(2/2)

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K	7	D	X	X	X	X	X	X	X	-	X	X	X	X	X	X	
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

16. Packing Type

- Common to all products, except of Mask ROM
- Divided into TAPE & REEL(In Mask ROM, divided into TRAY, AMMO Packing Separately)

Divide	Packing Type	New Marking
Component	TAPE & REEL	T
	Other (Tray, Tube, Jar)	0 (Number)
	Stack	S
Component (Mask ROM)	TRAY	Y
	AMMO PACKING	A
Module	MODULE TAPE & REEL	P
	MODULE Other Packing	M

17~18. Customer "Customer List Reference"