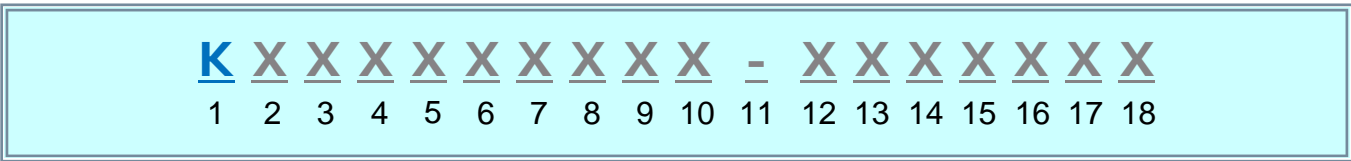




# High Speed SRAM Code Information(2/4)

Last Updated : May 2007



**1. Memory (K)**

**2. Sync SRAM : 7**

**3. Small Classification**

- A : Sync Pipelined Burst
- B : Sync Burst
- D : Double Data Rate
- I : Double Data Rate II, Common I/O
- J : Double Data Rate II, Seperate I/O
- K : Double Data Rate II+, Common I/O
- M : Sync Burst + NtRAM
- N : Sync Pipelined Burst + NtRAM
- P : Sync Pipe
- Q : Quad Data Rate I
- R : Quad Data Rate II
- S : Quad Data Rate II+

**4~5. Density**

- |          |         |
|----------|---------|
| 16 : 16M | 20 : 2M |
| 32 : 32M | 40 : 4M |
| 64 : 64M | 80 : 8M |

**6~7. Organization**

- |          |          |
|----------|----------|
| 08 : x8  | 09 : x9  |
| 18 : x18 | 32 : x32 |
| 36 : x36 |          |

**8~9. Vcc, Interface, Mode**

- 00 : 3.3V, LVTTTL, 2E1D WIDE
- 01 : 3.3V, LVTTTL, 2E2D WIDE
- 09 : 3.3V, LVTTTL, Hi SPEED
- 25 : 3.3V, LVTTTL, SB-FT WIDE
- 30 : 2.5/ 3.3V, LVTTTL, 2E1D
- 31 : 2.5/ 3.3V, LVTTTL, 2E2D
- 35 : 2.5/ 3.3V, LVTTTL, SB-FT
- 45 : 2.5V, LVTTTL, 2E2D
- 49 : 2.5V, LVTTTL, Hi SPEED
- 62 : 2.5V/ 1.8V, HSTL, Burst2
- 64 : 2.5V/ 1.8V, HSTL, Burst4
- 66 : 2.5V, HSTL, R-R
- 71 : 2.5V, HSTL, 3-1-1-1
- 74 : 1.8V/ 2.5V, HSTL, All
- 82 : 1.8V, HSTL, Burst2
- 84 : 1.8V, HSTL, Burst4
- 88 : 1.8V, HSTL, R-R
- T2 : 1.8V, 2 clock latency, Burst2
- T4 : 1.8V, 2 clock latency, Burst4
- U2 : 1.8V, 2.5 clock latency, Burst2
- U4 : 1.8V, 2.5 clock latency, Burst4

**10. Generation**

- M : 1st Generation
- A : 2nd Generation
- B : 3rd Generation
- C : 4th Generation

**11. "—"**

# High Speed SRAM Code Information(3/4)

Last Updated : May 2007

<u>K</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	-	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

## 12. Package

H : BGA, FCBGA, PBGA  
 G : BGA, FCBGA, PBGA (Lead-Free)  
 E : FBGA (Lead-Free)  
 F : FBGA  
 P : (L)QFP (Lead-Free)  
 Q : (L)QFP  
 C : CHIP BIZ  
 W : WAFER

## 13. Temp, Power

### - COMMON (Temp, Power)

C : Commercial, Normal  
 I : Industrial, Normal

### - WAFER, CHIP BIZ Level Division

0 : NONE, NONE  
 1 : Hot DC sort  
 2 : Hot DC, selected AC sort

## 14~15. Speed

### - Sync Burst, Sync Burst

65 : 6.5ns	75 : 7.5ns
80 : 8ns	85 : 8.5ns

### - Sync Burst + NtRAM

0 : NONE	10 : 10ns
31 : 312MHz	43 : 4.3ns
48 : 4.8ns	50 : 5ns
55 : 5.5ns	60 : 6ns
65 : 6.5ns	70 : 7ns
75 : 7.5ns	80 : 8ns
85 : 8.5ns	90 : 9ns

### - Other Small Classification (Clock Cycle Time)

10 : 100MHz	11 : 117MHz
13 : 133MHz	14 : 138MHz
16 : 166MHz	20 : 200MHz
25 : 250MHz	30 : 300MHz
33 : 333MHz	35 : 350MHz
37 : 375MHz	40 : 400MHz
45 : 450MHz	50 : 500MHz

### - Mode is R-L (Clock Access Time)

65 : 6.5ns

# High Speed SRAM Code Information(4/4)

Last Updated : May 2007

<b>K</b>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>-</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	<u>X</u>	
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18

## 16. Packing Type

- Common to all products, except of Mask ROM
- Divided into TAPE & REEL(In Mask ROM, divided into TRAY, AMMO Packing Separately)

Divide	Packing Type	New Marking
<b>Component</b>	TAPE & REEL	T
	Other ( Tray, Tube, Jar )	0 ( Number)
	Stack	S
<b>Module</b>	MODULE TAPE & REEL	P
	MODULE Other Packing	M

## 17~18. Customer "Customer List Reference"