

SERIAL PRESENCE DETECT

M470T6554EZ3-CE6/CD5/CCC

Organization :64M x 64
 Composition :32M x 16 * 8ea
 Used component part # :K4T51163QE-ZCE7/D6/E6/D5/CC
 # of rows in module2 Row
 # of banks in component :4 banks
 Feature :30mm height & double sided component
 Refresh :8K/64ms
 Bin Sort : E7(DDR2-800@CL=5), D6(DDR2-667@CL=4), E6(DDR2-667@CL=5), D5(DDR2-533@CL=4), CC(DDR2-400@CL=3)

Contents :

Byte #	Function described	Function Supported			Hex Value			Note
		CE6	CD5	CCC	CE6	CD5	CCC	
0	# of Serial PD Bytes written during module production	128bytes			80h			1
1	Total Number of SPD memory device	256bytes(2k bit)			08h			2
2	Fundameatal memory type	DDR2 SDRAM			08h			
3	# of row address on this assembly	13			0Dh			
4	# of column address on this assembly	10			0Ah			
5	# of module rows on this assembly	2 Row, Planar, 30.0mm			61h			
6	Data width of this assembly	64bits			40h			
7	Reserved	-			00h			
8	Voltage interface level of this assembly	SSTL 1.8V			05h			
9	DDR2 SDRAM cycle time at Max. Supported CAS latency=X	3.0ns	3.75ns	5.0ns	30h	3Dh	50h	3
10	DDR2 SDRAM Access time from clock at CL=X	+/-0.4	+/-0.5	+/-0.6	45h	50h	60h	
11	DIMM configuration type (address&command parity, data parity, ECC)	Non parity/ECC			00h			
12	Refresh rate	7.8us			82h			3,4
13	Primary DDR2 SDRAM width	x16			10h			
14	Error checking DDR2 SDRAM data width	N/A			00h			
15	Reserved	-			00h			
16	DDR2 SDRAM device attributes : Burst lengths supported	4,8			0Ch			
17	DDR2 SDRAM device attributes : # of banks on each DDR2 SDRAM device	4 banks			04h			3
18	DDR2 SDRAM device attributes : CAS latency supported	5,4,3			38h			3
19	DIMM Mechanical Characteristics	X =< 4.10			01h			
20	DIMM type information	SODIMM			04h			3
21	DDR2 SDRAM module attributes	Analysis probe not installed, FET switch external not enable			00h			
22	DDR2 SDRAM device attributes : General	Supports weak driver, 50Ohm ODT, PASR			07h			
23	DDR2 SDRAM cycle time at CL= X-1	3.75ns		5.0ns	3Dh	50h		3
24	DDR2 SDRAM access time from clock at CL= X-1	+/-0.5ns		+/-0.6	50h	60h		
25	DDR2 SDRAM cycle time at CL= X-2	5.0ns			50h			3
26	DDR2 SDRAM access time from clock at CL= X-2	+/-0.6ns			60h			
27	Minimum row precharge time(=tRP)	15ns			3Ch			3
28	Minimum row active to row active delay(=tRRD)	10ns			28h			3
29	Minimum RAS to CAS delay(=tRCD)	15ns			3Ch			3
30	Minimum active precharge time(=tRAS)	45ns		40ns	2Dh	28h		
31	Module rank density	256MB			40h			
32	Command and address setup time before clock(=tIS)	0.20ns	0.25ns	0.35ns	20h	25h	35h	3
33	Command and address hold time after clock(=tIH)	0.27ns	0.37ns	0.47ns	27h	37h	47h	3
34	Data input setup time before strobe(=tDS)	0.10ns		0.15ns	10h	15h		3
35	Data input hold time after strobe(=tDH)	0.17ns	0.22ns	0.27ns	17h	22h	27h	3
36	Write recovery time(=tWR)	15ns			3Ch			3

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Byte #	Function described	Function Supported			Hex Value			Note
		CE6	CD5	CCC	CE6	CD5	CCC	
37	Internal write to read command delay(=tWTR)	7.5ns		10.0ns	1Eh	28h		3
38	Internal read to precharge command delay(=tRTP)	7.5ns			1Eh			3
39	Memory analysis probe characteristics	-			00h			
40	Extension of Byte41 tRC and Byte42 tRFC	-			00h			
41	DDR2 SDRAM device min. active to active/auto refresh time(=tRC)	60ns		55ns	3Ch	37h		3
42	DDR2 SDRAM device min. auto-refresh to active/auto-refresh command period(=tRFC)	105ns			69h			3
43	DDR2 SDRAM device max. device cycle time(=tCK max)	8ns			80h			3
44	DDR2 SDRAM device max. skew for DQS and associated DQ signals(=tDQSQ max)	0.24ns	0.3ns	0.35ns	18h	1Eh	23h	3
45	DDR2 SDRAM read data hold skew factor(=tQHS)	0.34ns	0.4ns	0.45ns	22h	28h	2Dh	3
46	PLL Relock Time	-			00h			
47-48	DT in SPD	-			00h			
49	High Temp. Self Refresh	support			03h			
50-61	IDD in SPD	-			00h			
62	SPD data revision code	Revision 1.2			12h			
63	Checksum for bytes 0-62	-			4Ch	90h	0Ah	
64	Manufacturer JEDEC ID code	Samsung			CEh			
65-71Manufacturer JEDEC ID code	Samsung			00h			
72	Manufacturing location	Onyang Korea			01h			3
73	Manufacturer Part #(Memory module)	M			4Dh			
74	Manufacturer part # (DIMM configuration)	4			34h			
75	Manufacturer part # (Data bits & Module type)	Blank			20h			
76Manufacturer part # (Data bits & Module type)	7			37h			
77Manufacturer part # (Data bits & Module type)	0			30h			
78	Manufacturer part # (Operating Voltage)	T			54h			
79	Manufacturer part # (Module depth)	6			36h			
80	Manufacturer part # (Module depth)	5			35h			
81	Manufacturer Part # (Refresh. # of rows in comp. & interface)	5			35h			
82	Manufacturer part # (composition component)	4			34h			
83	Manufacturer part # (Component revision)	E-die			45h			
84	Manufacturer part # (Package type)	Z			5Ah			
85	Manufacturer part # (PCB revision)	3			33h			
86	Manufacturer part # (Hyphen)	"-"			2Dh			
87	Manufacturer part # (Power)	C			43h			
88	Manufacturer part # (Minimum cycle time)	E	D	C	45h	44h	43h	
89	Manufacturer part # (Minimum cycle time)	6	5	C	36h	35h	43h	
90	Manufacturer part # (T.B.D)	Blank			20h			
91	Manufacturer Revision Code(For PCB)	3			33h			
92	Manufacturer Revision Code (For component)	E-die			45h			
93	Manufacturing Date (Year)	-			-			5
94	Manufacturing date (week)	-			-			5
95-98	Assembly serial #	-			-			
99-127	Manufacturer specific data(may be used in future)	Undefined			00h			6
128-255	Open for customer use	Undefined			-			6

- Note :**
- 1 . This will typically be programmed as 128 Bytes.
 - 2 . This will typically be programmed as 256 Bytes.
 - 3 . From Datasheet
 - 4 . High order bit is Self Refresh "flag". If set to "1", the assembly supports self refresh.
 - 5 . These bytes are programmed by code of Date Year & Date Week with BCD format
 - 6 . These bytes are Undefined and can be used for Samsung's own purpose