

Preliminary

Product Technical Brief

S3C6400

Rev 1.5, Jun. 2007

Overview

S3C6400 is a 16/32-bit RISC cost-effective, low power, high performance micro-processor solution for mobile phones and general applications.

To provide optimized H/W performance for the 2.5G & 3G communication services, S3C6400 adopts a 64/32-bit internal bus architecture and includes many powerful hardware accelerators for tasks such as motion video processing, display control and scaling. Integrated Multi Format Codec (MFC) supports encoding and decoding of MPEG4/H.263, H.264 and decoding of VC1. This H/W Encoder/Decoder supports real-time video conferencing and TV out for NTSC and PAL mode

The S3C6400 has an optimized interface to external memory capable of sustaining the demanding memory bandwidths required in high-end communication services. The memory system has dual DRAM and Flash/ROM external memory ports for parallel access. DRAM port can be configured to support mobile DDR or standard SDRAM.

Flash/ROM Port supports NAND Flash, NOR-Flash, OneNAND and ROM type external memory.

To reduce total system cost and enhance overall functionality, S3C6400 includes many hardware peripherals such as camera interface, TFT 24-bit true color LCD controller, System Manager for power management, CF+, ATA I/F, 4-channel UART, 32-channel DMA, 4-channel Timers, General I/O Ports, IIS, IIC-BUS interface, USB 2.0 OTG operating at high speed(480Mbps), SD Host & High Speed Multi-Media Card Interface and PLLs for clock generation.

POP (Package on Package) option with MCP is available for small form factor applications.

This document contains specification and information under development.

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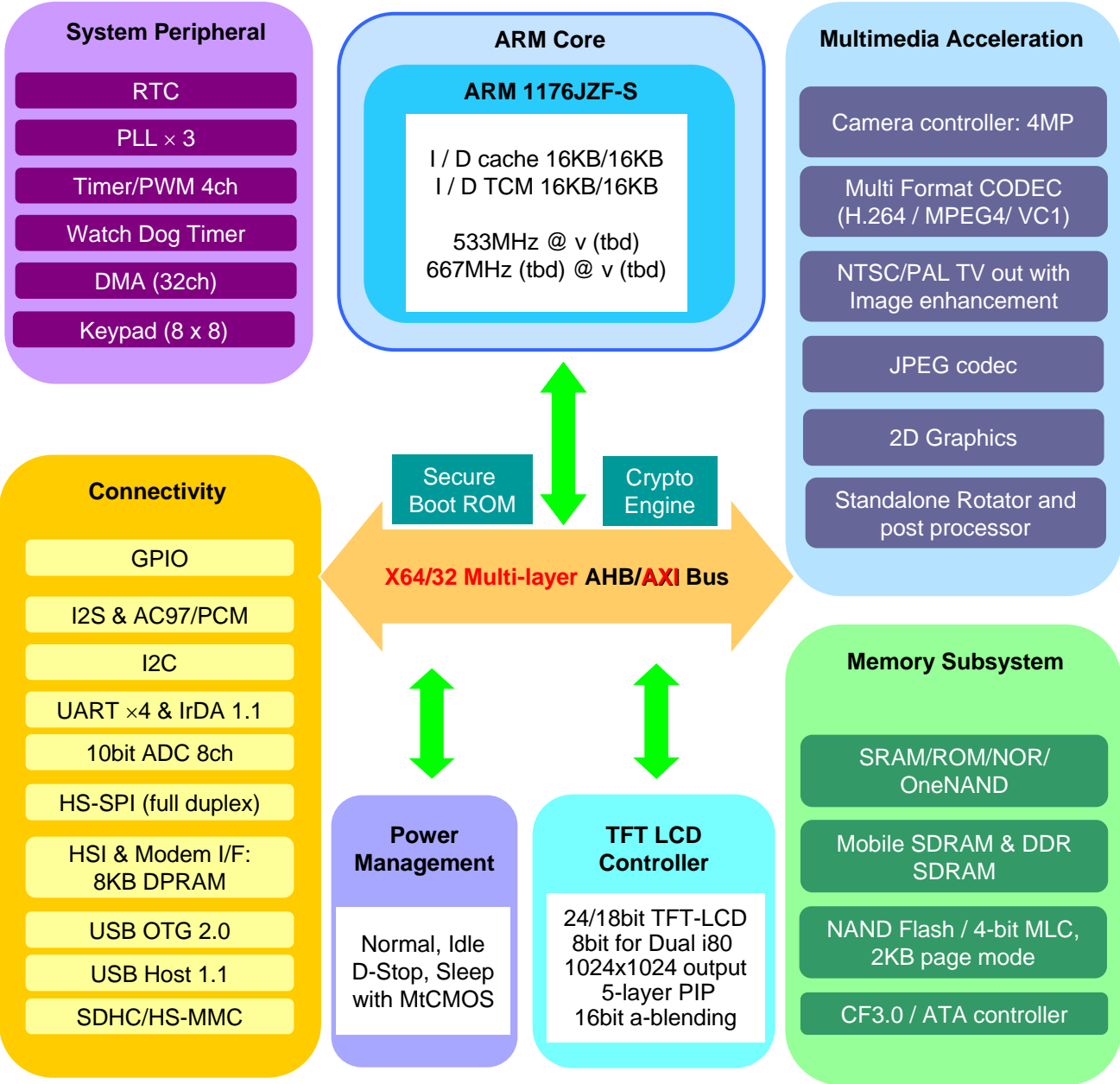
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Features Summary

- ARM1176JZF-S based CPU Subsystem with Java acceleration Engine
- 16/16KB I/D Cache, 16/16KB I/D TCM
- 533/667MHz Operating Frequency at TBD V and TBD V respectively.
- One 8-bit ITU 601/656 Camera Interface up to 4M pixel for scaled and 16M pixel for un-scaled resolution
- Multi Format CODEC provides encoding and decoding of MPEG-4/H.263/H.264 >30fps@SD/D1 and decoding of VC1 video >30fps@SD/D1
- 2D Graphics Acceleration with BitBlit and Rotation
- AC-97 audio codec interface and PCM serial audio interface
- 1/2/4/8 bpp Palletized or 8/16/24bpp Non-Palletized Color-TFT support up to 1024x1024
- I2S, I2C interface support
- Dedicated IrDA 1.1 port
- Configurable GPIOs
- On-chip USB 2.0 OTG supporting high speed(480Mbps, on-chip transceiver)
- On-chip USB 1.1 Host supporting full speed(12Mbps, on-chip transceiver)
- HS-MMC/SDHC card support
- CF+ and CompactFlash Spec 3.0 compatible (except MDMA operation)
- Real time clock, PLL, timer with PWM and watch dog timer
- 32 channel DMA controller
- Support 8X8 key matrix
- Advanced power management for mobile applications
- Memory Subsystem
 - SRAM/ROM/NOR Interface with x8 or x16 data bus
 - Muxed OneNAND Interface with x16 data bus
 - NAND Flash Interface with x8 data bus with 1/4-bit hardware ECC circuit
 - SDRAM Interface with x16 or x32 data bus
 - Mobile SDRAM Interface with x16 or x32 data bus (133Mbps/pin rate)
 - Mobile DDR Interface with x16 or x32 data bus (266Mbps/pin DDR)

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Product Details

ARM Core

- The ARM1176JZF-S processor incorporates ARM V6 architecture. It supports the ARM and Thumb™ instruction sets, and Jazelle technology for direct execution of Java byte codes.
- A range of SIMD DSP instructions that operate on 16-bit or 8-bit data values in 32-bit registers.
- ARM1176JZF Features
 - TrustZone™ security extensions
 - S/W Driven Power Management
 - High-speed Advanced Microprocessor Bus Architecture (AMBA) Advanced
 - Extensible Interface (AXI) level two interfaces supporting prioritized multiprocessor implementations.
 - Integer unit with integral Embedded ICE-RT logic
 - Eight-stage pipeline
 - Branch prediction with return stack
 - Low interrupt latency configuration
 - External coprocessor interface and coprocessors CP14 and CP15
 - Instruction and Data Memory Management Units (MMUs), managed using MicroTLB structures backed by a unified Main TLB
 - Instruction and data caches, including a non-blocking data cache with Hit-Under-Miss (HUM)
 - Virtually indexed and physically addressed caches
 - 64-bit interface to both caches
 - DMA
 - Vector Floating-Point (VFP) coprocessor support
 - External coprocessor support
 - Trace support
 - JTAG-based debug

Memory Subsystem

- SRAM/ROM/NOR Interface
 - x8 or x16 data bus
 - Address range support: 26-bits(64MB)
 - Support byte and half-word access
- Muxed OneNAND Interface
 - x16 data bus
 - Support byte and half-word access
- SDRAM Interface
 - X16, x32 data bus
 - 1.8V interface voltage
 - Density support : up to 1Gb
 - x16 data bus with 133Mbps/pin data rate
 - Mobile SDRAM feature support :
 - DS (Driver Strength Control)
 - TCSR (Temperature Compensated Self-Refresh Control)
 - PASR (Partial Array Self-Refresh Control)
- Mobile DDR Interface
 - x16, x32 data bus with 266Mbps/pin double data rate (DDR)
 - 1.8V interface voltage
 - Density support : up to 1Gb
- NAND Flash Memory for boot loader and data storage
 - System can be booted from NAND when system initialization begins
 - Rest of memory area is used for storing user data
- NAND Interface
 - Support industry standard NAND interface
 - 1/4-bit hardware ECC circuit
 - x8 data bus

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□ Multimedia Acceleration

■ Camera Interface

- 8-bit ITU-R601/ITU-R656 format input
- Up to 4M pixel for scaled or 16M pixel for un-scaled resolution
- YCrCb 4:2:2 to 4:2:0 down-sampling, down-scaling for MPEG and JPEG
- RGB 24-bit or 16-bit output for preview
- Image windowing and zoom-in function
- Test pattern generation
- Image flip supports Y-mirror, X-mirror, 180° rotation
- H/W Color Space Conversion
- LCD controller direct path supported
- Image effect supported

■ Multi Format CODEC (MFC)

- Real-time Video Encoding & decoding of MPEG4/H.263/H.264 and decoding of WMV9
- MPEG4 Up to Simple Profile : 30fps@SD(720x480)
- Supports H.263 Baseline 30fps@SD(720x480)
- H.264 Baseline Profile Level 3.0 : 30fps@SD(720x480)
- VC1 Decoding : 30fps@SD(720x480)

■ JPEG Codec

- Compression/decompression up to 65536 x 65536
- Encoding format: YCbCr4:2:2 or YCbCr4:2:0
- Decoding format: YCbCr4:4:4, YCbCr4:2:2, YCbCr4:2:0 or Gray

■ Rotator

- Supported image format : YCbCr 4:2:2(interleave), YCbCr 4:2:0 (non-interleave), RGB565 and RGB888(unpacked)
- Supported rotate degree : 90, 10, 270, flip vertical and flip horizontal
- Supported image size : 2048 x 2048

■ 2D Graphic Accelerator

- Primitive drawing engine
 - Line/Point drawing
 - Bit Block Transfer (BitBLT)
 - Color expansion: Text drawing
- Per-pixel operation (max 2048x2048 resolution)
 - 90°/180°/270°/X-flip/Y-flip rotation
 - Window clipping
 - Rasterization
 - 256-level per-pixel alpha blending

■ TV(NTSC/PAL) Encoder with Image Enhancer

- Out Video Format : NTSC-M/PAL-B,D,G,H,I Compliant
- Macrovision for anti-taping (Version 7.1.L1)
- Support source format : YCbCr420/422, RGB 16/18/24
- Built in the MIE (Mobile Image Enhancer) Engine
- Black & White Stretch
- Blue Stretch & Flesh-Tone Correction
- Dynamic Horizontal Peaking & LTI
- Black and White Noise Reduction
- Original, Full Size, Wide Size Video-Out

■ Video Post Processor

- Video input format conversion
- Video/Graphic scaling up/down or zooming in/out
- Color space conversion from YCbCr to RGB
- Color space conversion from RGB to YCbCr
- Dedicated local interface for display
- Dedicated Scaler for TV Encoder

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□ Display Controller

- Support 24/18 bit RGB Interface LCD
- Support 8/6 bit RGB Interface
- Support Dual i80 Interface LCD
- 1/2/4/8bpp Palletized or 8/16/24-bpp Non-Palletized Color-TFT support
- 320X240, 640x480 or other display resolutions up to 1024x1024
- Max. 2K x 2K virtual screen size
- Support 5 Window Layer for PIP or OSD
- Realtime overlay plane multiplexing
- Programmable OSD window positioning
- 16-level alpha blending

□ Security Subsystem

■ On-Chip secure boot ROM

- 32KB secure boot ROM for secure boot

■ H/W Crypto Accelerator

- Securely integrated AES, DES/3DES, SHA-1/MD5, RNG

■ ARM TrustZone™

- Enabling enhanced secure platform for separate (secure/non-secure) execution environment for security sensitive application

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□ Connectivity

■ I2S Bus Interface

- 2-ch IIS-bus for the audio-codec interface with DMA-based operation
- Serial, 8/16-bit per channel data transfers
- Supports IIS, MSB-justified and LSB-justified data format
- 16, 24, 32, 48 fs of bit clock frequency
- 256, 384, 512, 768 fs of codec clock frequency

■ PCM Audio I/F

- 16-bit mono audio I/F
- Master mode only

■ AC97 Audio I/F

- Independent channels for stereo PCM In, stereo PCM Out, mono MIC In.
- 16-bit stereo(2-channel) audio.
- Variable sampling rate AC97 Codec interface (48KHz and below)

■ Modem I/F

- Asynchronous direct and indirect 16-bit SRAM-style interface (support i80 style)
- On-chip 8KB dual-ported SRAM buffer for direct interface
- On-chip Write/Read FIFO (each 288-word) to support indirect burst transfer

■ HSI

- MIPI Standard Draft Compliant
- High speed synchronous serial interface

■ CF+/ATA controller

- CF+ and CompactFlash Spec 3.0 compatible including ATA6 (except MDMA operation)

■ I2C Bus Interface

- 1-ch Multi-Master IIC-Bus
- Serial, 8-bit oriented and bi-directional data transfers can be made at up to 100 Kbit/s in the standard mode
- Up to 400 Kbit/s in the fast mode

■ UART

- 4-channel UART with DMA-based or interrupt-based operation
- Supports 5-bit, 6-bit, 7-bit, or 8-bit serial data transmit/receive
- Supports external clock for the UART operation (UCLK)
- Programmable baud rate
- Loop back mode for testing
- Non-integer clock divides in Baud clock generation (BRM)

■ IrDA

- IrDA v1.1 support (1.152Mbps and 4Mbps)
- SIR(111.5kbps) mode is supported by the UART IrDA 1.0 block
- Internal 64-byte Tx/Rx FIFO

■ USB OTG 2.0

- Complies with the USB OTG 2.0
- Supports high speed up to 480Mbps
- On-chip USB transceiver

■ USB Host 1.1

- Complies with the USB 1.1
- Supports full speed up to 12Mbps
- On-chip USB transceiver

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■ HS-MMC/SDIO

- Multimedia Card Protocol version 4.2 compatible (HS-MMC)
- SD/SDIO Memory Card Protocol version SDA spec version 2.0 compatible
- SDHC (SD High Capacity) card support
- DMA based or Interrupt based operation
- 512 Bytes (HS-MMC) and 64 Bytes (MMC) FIFO for Tx/Rx: 128 word FIFO for Tx/Rx
- CE-ATA support
- 3-ch SD/SDIO or
- 1-ch HS-MMC & 1x SD/SDIO

■ SPI Interface

- 2-ch Serial Peripheral Interface Protocol with full-duplex: up to 50Mbps
- DMA-based or interrupt-based operation

■ Keypad

- 8x8 Key Matrix support
- Provides internal de-bounce filter

■ A/D Converter and Touch Screen Interface

- 8-ch multiplexed ADC
- Max. 500Ksamples/sec and 10bit resolution

■ Configurable GPIO (TBD)

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□ System Peripheral

■ Real Time Clock

- Full clock features: sec, min, hour, date, day, week, month, year
- 32.768 KHz operation
- Alarm interrupt
- Time-tick interrupt

■ PLL

- Three on-chip PLLs, APLL/ MPLL / EPLL
- APLL dedicates to ARM core
- MPLL generates the system reference clock
- EPLL generates clocks for the audio interface

■ Timer with Pulse Width Modulation

- 4-ch 32-bit Timer with PWM
- 1-ch 32-bit internal timer with DMA-based or interrupt-based operation
- Programmable duty cycle, frequency, polarity
- Dead-zone generation
- Support external clock source

■ 16-bit Watch Dog Timer

■ DMA

- 4 General DMA embedded. 8 channel supported per each DMA so then totally 32 channel is supported
- Memory to memory, IO to memory, memory to IO, and IO to IO support
- Burst transfer mode to enhance the transfer rate

■ Vectored Interrupt Controller

- multiple interrupt request inputs, one for each interrupt source, and one interrupt request output for the processor interrupt request input
- software can mask out particular interrupt requests
- prioritization of interrupt sources for interrupt nesting.

■ Power Management

- Clock-off control for individual components
- Various power-down modes are available such as Slow, Idle, Stop and Sleep mode
- Wake-up by one of external interrupts or by the RTC alarm interrupt

□ Electrical Characteristics

■ Operating Conditions

- Supply Voltage for Logic Core: TBD V
- External Memory Interface: 1.8V ~ 2.5V (tbd)
- External I/O Interface: 1.8 V ~ 3.3V (tbd)

■ Operational core frequency

- 400MHz @TBD V
- 533MHz @TBD V

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Package

- Support POP with MCP
 - 2Gb OneNAND, 512Mb mDDR SDRAM, TBD pins 14X14mm 1.4T
 - 1Gb NAND, 512Mb OneDRAM, 512Mb mDDR SDRAM,