Samsung Foundry

Design Enablement for Advanced Technologies

Smart & Innovative Foundry Solution
Contents

- Landscape
  - Market Trends

- Readiness of Design Enablement
  - 32nm/28nm Design Enablement

- Exploring Design Challenges in advanced process
  - Technology Trends
  - Solutions

- Conclusion

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Market Trends

Digital Convergence, Smart Information Hub ...

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Mobile SOC Design Trends

Required Mobile SOC Spec.

- Mobile CPU
  - > 10,000 DMIPS

- DRAM Bandwidth
  - > 20GB/sec

- Multimedia Contents
  - > Full HD 1080P (3D & 3D GFX)

Bottleneck of Mobile SOC Design

- High Performance, Low Power
- Better Packaging
32/28nm Design Enablement
Samsung supports a comprehensive PDK (Process Design Kit)

- Major EDA tools are available from Design Enablement Partners

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<th>Synopsys</th>
<th>Cadence</th>
<th>Mentor Graphics</th>
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<tr>
<td>SPICE</td>
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<td>DRC</td>
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Samsung supports **Product Proven Library IP** in 32nm and 28nm

### Standards Cells
- sLVT(SG)
- LVT (SG)
- RVT (SG)

### Memory
- SP SRAM (RA1)
- DP SRAM (RA2)
- 1P Reg. File (RF1)
- 2P Reg. File (RF2)
- Via-1 ROM (VROM)

### GPIO
- 1.2V~1.8V GPIO
- 1.8V~3.3V GPIO

**32LP / 28LPP**

**HD(L)** High Density (Low Voltage)
**HS(L)** High Speed (Low Voltage)
**LP** Low Power

**HD/HS/HSL**
**HD/HDL**
**HD/HS/HSL**
**HD/HS/HSL**

**HD**
**HD**
**HSL**

**EG + SG_RVT**
**EG + SG_RVT**
Collaboration is delivering industry leading solutions

**Excellence** in essential building blocks for contemporary SOCs

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**From analog to processor cores**

**Various silicon proven IP**

- **Processor Cores**
  - ARM7/9/11 Series
  - Cortex M/R/A Series

- **System IP**
  - Interconnect IP
  - Memory controllers
  - System Controllers
  - Peripherals
  - CoreSight

- **High Speed Interface IP**
  - SATA, PCIe
  - USB2/3, HSIC
  - LVDS, mini-LVDS, sub-LVDS
  - MIPI D/M-PHY
  - HDMI, DisplayPort

- **Multimedia IP**
  - JPEG Codec
  - NTSC/PAL encoder

- **Memory**
  - (HD/HS/LP)SRAM, VROM
  - eFuse, OTP

- **Embedded Memory**
  - ADC, DAC, AFE
  - PLL
  - Audio CODEC
  - Temp sensor, LDO

- **Memory Interface**
  - DDR2/3, LPDDR2/3

- **I/O**
  - In-line, staggered, multi-row
  - Wide-range GPIO

- **Standard Cell Library**
  - HD/HS
  - Multi Vth
  - Multi channel length
  - Power management kit

- **Mixed-Signal Core**
  - DDR2/3, LPDDR2/3

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**Samsung DFM**

Samsung supports **an integrated DFM methodology** in 32nm and 28nm.

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<th>Family</th>
<th>Kit</th>
<th>IP</th>
<th>Chip</th>
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<td>32/28nm</td>
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<td><strong>Rule-based Verification</strong></td>
<td>DRC</td>
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<td>LUP (Litho Unfriendly Pattern)</td>
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<td>PHC pattern matching (Process Hotspot Check)</td>
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<td>MCD/MAS (Recommended Rule Deck)</td>
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<td>VIA</td>
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<td><strong>Model-based Verification</strong></td>
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<td>FLHC (Fast Litho Hotspot Checker)</td>
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<td>CMP</td>
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<td>CAA</td>
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<td><strong>Layout Enhancement</strong></td>
<td>LUP-enabled router</td>
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<td>PHR (Process Hotspot Repair)</td>
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<td>Dummy Fill</td>
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*M: Mandatory, R: Recommend*
Samsung Design Methodology

- Samsung DM has been enabling the world’s best in-class products.

**World 1st 1GHz Mobile Application Processors (S5PC110) at 1.2V in 45nm LP Process**
Announced on Sept. 22nd, 2009

- 45nm Low power process
- Multi-V_{th} for power-performance opt.
- Aggressive process migration plan
- Over 7 hours of video playback: isolated power domain & bus architecture, dynamic on/off scheme

**World’s 1st Mobile Application Processors in 32nm HK/MG Process**
Announced at 2010 SMF (Taipei, Taiwan, Sept. 7th, 2010)

- 32nm Low power process
- Multi-V_{th}/LLP for power-performance opt.
- Successful low power DM migration (PG, MVDD, ABB, etc.)
- Statistical timing/power analysis added
- Unified LP design flow

Paradigm Shift
Deterministic → Statistical(μ, σ)

Pessimism reduction by using SSTA

Relative Margin for SSTA vs. Margin, AOCVM
Technology Trends and Design Challenges
Process Technology Trends

- 65nm
- 45nm
- 32/28nm
- 20nm
- 14nm

- Strained Si
- ULK
- Gate First
- Gate Last
- FinFET

- ISDA joint development
- Running in very high volumes
- Fueling the mobile generation

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Design Challenges

- New patterning (DP, TP, and SADP)
- Complex ground and recommended rules
- 3D Transistor (FinFET) structure
- Scaled BEOL with new material
- Ever increasing on-chip variation
- FEOL/BEOL reliability characteristics

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20nm Design Enablement - Challenges & Solutions
Key Technology Challenges

- Collaborate for optimal solutions

![Diagram showing double patterning and lithography techniques](image)

**32/28nm vs 20nm**
- Metal Pitch: 90nm (1X)
- # of Routing Rules: 242 (45nm), 306 (32nm), 574 (20nm)

**Double Patterning (DP) Awareness**
- DP rules
- DP-compliant IPs
- DP-aware routing
- DP rule checking

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14nm Design Enablement - Challenges & Solutions
Key Technology Challenges

Technical Challenges

- 2D → 3D Device Modeling
- 2D → 3D Parasitic Extraction
- Process Variability Increase
- Continuous → Discrete Transistor Width ("Quantized width")
- Fine bit-cell control (1:1.2:1.5) → Coarse bit-cell Control (1:1;1, 1:2:2) in SRAM

How to solve it

- BSIM-CMG Model as a CMC Standard
- Extraction tool enhancement with High Accuracy (C: < +/-5%, R: < +/-3%)
- Statistical-based process-tolerant design
- Optimal Fin architecture through coarse-grain circuit optimization
- FinFET-optimized Read/Write assist introduction in SRAM

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Conclusion

Product Proven Design and Process Technology in 32nm/28nm

- High-K/Metal Gate
- PDK / Library / IP / Design Methodology

Solutions for Advanced Technology Leadership

- Double Pattern
- 3D Transistors

Providing Comprehensive Enablement to meet customer needs

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Thank You