Samsung Foundry’s 32/28nm Low-Power (LP) Gate First High-k Metal Gate (HKMG) process node offers considerable power and performance advantages to a growing spectrum of mobile and IT infrastructure computing applications.

Virtually all mobile applications relying on batteries and extremely tight power budgets demand 32/28nm LP solutions. But, low-power solutions are no longer limited to mobile applications. Reducing power is now a concern across a wide set of applications such as communications, networking, servers, and data centers.

Advances in Material Science

As conventional Poly/SiON reached its limits, HKMG was introduced to continue gate dielectric scaling (Tox/Tinv). The 32/28nm LP HKMG integration achieved an array of benefits and improvements over 45nm LP Poly/SiON, including:

- 2x gate density increase (Superior area scaling with Gate-First HKMG)
- >100x lower gate leakage
- >40% delay improvement at fixed leakage
- ~10x leakage reduction at fixed speed
28nm Migration Path
Before its introduction, Samsung Foundry invested two years of development to fine tune its 32nm LP HKMG process technology node. Consequently, Samsung has achieved a full cycle of valuable HKMG learning and high-volume experience going into 28nm LP HKMG process technology.

With initial emphasis on 32nm LP, Samsung has simultaneously and aggressively placed resources on 28nm LP to create a remarkably simple migration path. All design rules at 32nm are shrinkable and can be easily migrated, allowing any 32nm design to be 28nm friendly. Samsung has also released all beta models of its design kits and SPICE models for 28nm. Leading-edge customers can download the latest SPICE models and design kits to start designing at 28nm.

Complete Designing Ecosystem
Samsung’s 32/28nm process nodes are well supported by a full-featured suite of IP libraries from ARM®, Samsung’s primary IP library provider. The Samsung-ARM relationship has spanned over several previous generations and will continue to support Samsung Foundry.

Plus, Samsung provides extensive DFM solutions validated on its technology. As for design flows, partnerships are forged with leading EDA tool vendors like Synopsys®, Cadence®, Mentor Graphics®, and Magma®. Their design flows are validated on Samsung’s 32/28nm technologies. The bottom line for customers is a wide range of highly comprehensive choices from which to select.

Industry’s First Foundry High-K Metal Gate Technology
HKMG process technology involves two distinctly different integration flows, namely Gate-First and Gate-Last. In a Gate-First approach, the transistor’s gate stack is fabricated first, followed by the source and drain, very much like traditional CMOS transistor architecture. A Gate-Last process is just the opposite, a sacrificial gate stack is stripped away after source and drain implantation followed by a replacement gate fabrication. Samsung together with its Common Platform (CP) and International Semiconductor Development Alliance (ISDA) partners have defined HKMG process technology to provide what is best for customer.

For 32/28nm, Samsung and its partners were the first to introduce the Foundry HKMG strategy. At 32/28nm, a Gate-First HKMG was selected since the scheme has proven to meet market and customer needs achieving superior area scaling and preservation of layout styles without complex restricted design rules. Also, customers can take advantage of a more cost-effective HKMG process scheme due to its compatibility with conventional transistor gate process integration. Moving forward to 20nm and below, Samsung Foundry and its partners have conducted extensive HKMG R&D to ensure the right technologies are deployed to the customer and market challenges are different from 32/28nm and technology primarily dominated by sub-90nm lithography patterning challenges so litho-dominated restricted design rules are required to extend 193nm Immersion Lithography. A Gate-Last scheme has been deemed the best for optimal strain engineering necessary to meet performance even for Low-Power technology. In addition, other advanced technologies such as middle-of-line local interconnects and aggressive lithography RET have also been employed and tuned to attain superior customer design scaling at the new node.