

DDR2 SDRAM Module Code Information (1/2)

Last Updated : August 2009

M X X X **T** X X X X X X X - X X X X X
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18

1. Memory Module(M)

2. Module Configuration

3 : DIMM
4 : SODIMM

3~4. Data bit

78 : x64 240pin Unbuffered DIMM
91 : x72 240pin ECC Unbuffered DIMM
92 : x72 240pin VLP Registered DIMM
93 : x72 240pin Registered DIMM
95 : x72 240pin Fully Buffered DIMM
70 : x64 200pin Unbuffered SODIMM

5. DRAM Component Type

T : DDR2 SDRAM (1.8V VDD)

6~7. Depth

32 : 32M
33 : 32M (for 128Mb/ 512Mb)
64 : 64M
65 : 64M (for 128Mb/ 512Mb)
28 : 128M
29 : 128M (for 128Mb/ 512Mb)
56 : 256M
57 : 256M (for 512Mb/ 2Gb)
51 : 512M
52 : 512M (for 512Mb/ 2Gb)
1G : 1G
1K : 1G (for 2Gb)

8. # of bank in Comp., Interface, Refresh

5 : 4bank, SSTL(1.8V, 1.8V), 64ms/ 8K (7.8us)
6 : 8bank, SSTL(1.8V, 1.8V), 64ms/ 8K (7.8us)

9. Bit Organization

0 : x4
3 : x8
4 : x16
6 : x4 Stack (JEDEC Standard)
7 : x8 Stack (JEDEC Standard)
8 : x4 Stack
9 : x8 Stack

10. Component Revision

M : M-die
A : A-die
B : B-die
C : C-die
D : D-die
E : E-die
F : F-die
G : G-die
Q : Q-die
R : R-die

11. Package

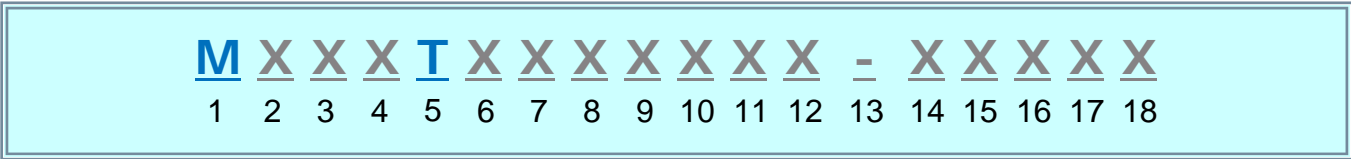
Z : FBGA (Lead-Free)
J : FBGA (Lead-Free, DDP)
Q : FBGA (Lead-Free, QDP)
H : FBGA (Lead-Free & Halogen-Free)
M : FBGA (Lead-Free & Halogen-Free, DDP)
E : FBGA (Lead-Free & Halogen-Free, QDP)

12. Module Type & PCB Revision

0 : Mother PCB
1 : 1st Rev.
2 : 2nd Rev.
3 : 3rd Rev. (Dummy Pad PCB)
4 : 4th Rev.
A : Parity DIMM
S : Reduced PCB

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13. "—"

14. Temp & Power

C : Commercial Temp, Normal Power

L : Commercial Temp, Low Power

Y : Commercial Temp, Low Voltage

15~16. Speed

CC : DDR2-400 (200Mhz@CL=3, tRCD=3, tRP=3)

D5 : DDR2-533 (266Mhz@CL=4, tRCD=4, tRP=4)

E6 : DDR2-667 (333Mhz@CL=5, tRCD=5, tRP=5)

F7 : DDR2-800 (400Mhz@CL=6, tRCD=6, tRP=6)

E7 : DDR2-800 (400Mhz@CL=5, tRCD=5, tRP=5)

17. AMB Vendor for FBDIMM

5 : Intel

6, 8 : IDT

3, 4, 9 : Montage

18. Customer (Special Handling)

"Customer List Reference"