

# **DDR2 Application Note**

**User guide for using Parity DIMM on Non-parity system**

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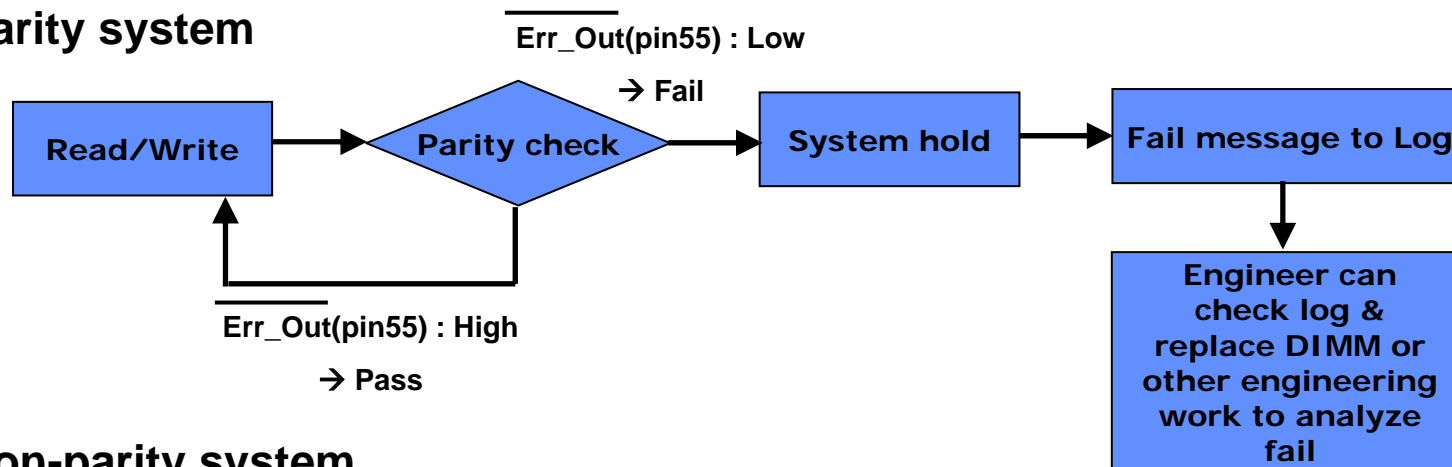
# Comparison of Parity vs Non-parity

- There's no difference between Parity RDIMM and Non-parity RDIMM except availability of parity function support.

Pin / Front side					Pin / Front side				
144	DQ21	54	NC	174	NC	87	V <sub>DD</sub>	187	V <sub>DD</sub>
145	V <sub>SS</sub>	55	NC/Err_Out	175	V <sub>DDQ</sub>	88	NC/Par_In	188	A0
146	DM2/DQS11	56	V <sub>DD</sub>	176	A12	89	V <sub>DD</sub>	189	V <sub>DD</sub>

Pin 55 (NC/Err\_Out) : Non-parity → No connect, Parity → Err\_Out (output / parity error found in Add.&Cont. bus)  
 Pin 68 (NC/Par\_in) : Non-parity → No connect, Parity → Par\_in (input / parity bit for Add.&Cont.bus)

- Parity system



- Non-parity system

- No way to detect error in memory access
- Even though there is any failure in CMD/ADDR, system will continue to operate but the output of this operation should be wrong

# How to use Parity DIMM on Non-parity system

Application  
Note

- ❑ There's no problem to operate the Parity RDIMM on non-parity application
- ❑ However, some old system BIOS can not read the Parity RDIMM during the initial booting(Only recognize the Non-parity RDIMM because of SPD)
- ❑ So, BIOS update can solve this booting problem
- ❑ Parity vs Non-parity in DDR2 SPD (JEDEC standard)

## Byte 11: DIMM Configuration Type

This byte describes the module's error detection and/or correction schemes on the data, address and command buses.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TBD	TBD	TBD	TBD	TBD	Address/Command Parity	Data ECC	Data Parity
0	0	0	0	0	1 or 0	1 or 0	1 or 0

1 = Supported on this assembly, 0 = Not supported on this assembly.  
Note: Data ECC includes Data Parity, therefore modules with Data ECC shall encode bit 1 as 1 and bit 0 as 0.

Parity : 00000110 = 06h / Non-parity : 00000010 = 02h

Even there's no need to change the BIOS, If parity function is disabled in SPD.  
Anyway, there should be a meaningless signal  
through the Pin55(Err\_out) of Parity RDIMM with this parity disabled.

❑ System level booting test of Parity RDIMM with Non-parity platform

Non-parity System	Chipset	Vendor	Board	Parity RDIMM DDR2 400	
				SPD Byte # 11 : 02h Parity disable	SPD Byte # 11 : 06h Parity support
Lindenhurst	A	A1	Pass	Fail	
	B	B1	Pass	Fail	
		B2	Pass	Pass	
		B3	Pass	Pass	
	C	C1	Pass	Pass	
Twin Castle	B	B4	Pass	Pass	
	C	C2	Pass	Pass	

There's no booting failure issue, If parity function is disabled in SPD.

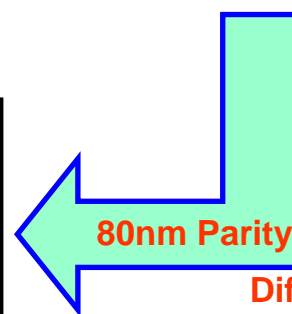
# Samsung Registered DIMM support status

Application  
Note

Type		Parity (DDR2-667/800)										Non-Parity (DDR2-400/533)									
Based Comp		512Mb				1Gb				2Gb		512Mb				1Gb				2Gb	
MDL Den		512	1GB		2GB	1GB	2GB		4GB	4GB	8GB	512	1GB		2GB	1GB	2GB		4GB	4GB	8GB
Conf.		1Rx8	2Rx8	1Rx4	2Rx4	1Rx8	2Rx8	1Rx4	2Rx4	2Rx8	2Rx4	1Rx8	2Rx8	1Rx4	2Rx4	1Rx8	2Rx8	1Rx4	2Rx4	2Rx8	2Rx4
90 nm	R/C	F	G	H	J	F	G	H	K stack	-	-	A	B	C	J	A	B	C	K	-	-
	REG	(32)866			866	866			868	-	-	(32)864								868	-



80 nm	R/C	F	G	H	L	F	G	H	L planar	G	K
	REG	(32)866			868	866			868		



80nm Parity RDIMM vs Non-parity RDIMM

Different Part number,  
But Using same gerber & reg.

From 80nm DDR2, Parity RDIMM will be supported with parity disable in SPD to Non-Parity application.

- 👉 There's almost no change for Non-parity user
- 👉 The only difference is using a parity register
- 👉 Do not use the pin55(NC/Err\_out) & 68(NC/Par\_in) and ignore the output signal of pin55(Err\_out)