

Application Note

ARM PrimeCell™ MPMC (PL172)

Register Setting for Mobile SDRAM

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Purpose

This application note will guide you to set up the registers for address mapping, MRS and EMRS of Mobile SDRAM using ARM PrimeCell™ MPMC (PL172). It describes how to calculate register values by different memory densities. This will be helpful to mobile system software engineers.

Definitions and Acronyms

Definitions and Acronyms	Description
MRS	Mode Register Setting
EMRS	Extended Mode Register Setting
MPMC	Multi Port Memory Controller
SDRAM	Synchronous DRAM

References

- ARM PrimeCell™ MPMC (PL172) Technical Reference Manual
- Samsung Mobile SDRAM Databook

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1 Case for 32-bits 256Mb (8Mx32)

According to the density variation of memory device, users should change 3 register configurations correctly, which are

- 1) MPMC_DY_CONFIG_WW__ADDRESS_MAPPING_VALUE,
- 2) MPMC_DY_MODE_REGISTER_ADDRESS_VALUE and
- 3) MPMC_DY_EXTENDED_MODE_REGISTER_ADDRESS_VALUE.

These registers are defined in header file, 'MPMC.h'.

As an example, sequences to calculate these register configuration values of 32-bits, 256Mb (8Mx32) will be shown below. Assume that CAS Latency is 2, Burst Length is 4, and that Drive Strength and PASR is full.

1.1 MPMC_DY_CONFIG_WW__ADDRESS_MAPPING_VALUE

In the PL172 Technical Reference Manual, Register Description for MPMCDynamicConfig shows address mapping value for each density of memory.

Table 1.1 MPMCDynamicConfig registers

[14]	[12]	[11:9]	[8:7]	Description
32-bit external bus low-power SDRAM address mapping (Bank, Row, Column)				
1	1	000	00	16Mb (2Mx8), 2 banks, row length = 11, column length = 9
1	1	000	01	16Mb (1Mx16), 2 banks, row length = 11, column length = 8
1	1	001	00	64Mb (8Mx8), 4 banks, row length = 12, column length = 9
1	1	001	01	64Mb (4Mx16), 4 banks, row length = 12, column length = 8
1	1	001	10	64Mb (2Mx32), 4 banks, row length = 11, column length = 8
1	1	010	00	128Mb (16Mx8), 4 banks, row length = 12, column length = 10
1	1	010	01	128Mb (8Mx16), 4 banks, row length = 12, column length = 9
1	1	010	10	128Mb (4Mx32), 4 banks, row length = 12, column length = 8
1	1	011	00	256Mb (32Mx8), 4 banks, row length = 13, column length = 10
1	1	011	01	256Mb (16Mx16), 4 banks, row length = 13, column length = 9
1	1	011	10	256Mb (8Mx32), 4 banks, row length = 13, column length = 8
1	1	100	00	512Mb (64Mx8), 4 banks, row length = 13, column length = 11
1	1	100	01	512Mb (32Mx16), 4 banks, row length = 13, column length = 10

Table 1.1 shows that the configuration value for 256Mb (8Mx32) is 0101 0111 0000 0000b, which can be converted to 0x5700.

Therefore MPMC_DY_CONFIG_WW_ADDRESS_MAPPING_VALUE is 0x5700.

1.2 MPMC_DY_MODE_REGISTER_ADDRESS_VALUE

Address mapping table is in the PL172 Technical Reference Manual, and the table below is for 32-bit 256Mb (8Mx32, BRC).

Table 1.2 Address Mapping Table for 32-bit 256Mb (8Mx32, BRC)

MPMC output address (MPMCADDRROUT)	Memory device connections	AHB address to row address	AHB address to column address
14	BA1	23	23
13	BA0	24	24
12	12	22	-
11	11	21	-
10	10/AP	20	AP
9	9	19	-
8	8	18	-
7	7	17	9
6	6	16	8
5	5	15	7
4	4	14	6
3	3	13	5
2	2	12	4
1	1	11	3
0	0	10	2

As you see in Table 1.2, memory address [0] is matched to AHB address [10]. MRS setting value is 0010 0010b for CL=2 and BL=4 as mentioned above. This will make address matching as shown in Table 1.3

Table 1.3 Address Matching for MRS

AHB Add	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Memory Add		8	7	6	5	4	3	2	1	0										
MRS Setting	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	0				8				8				0				0			

Therefore, MPMC_DY_MODE_REGISTER_ADDRESS_VALUE is 0x8800.

1.3 MPMC_DY_EXTENDED_MODE_REGISTER_ADDRESS_VALUE

Since PASR and Drive Strength are full, all bits except BA1 must be set to 0 for EMRS. See Table 1.2, BA1 is matched to AHB address [23]. Remember that the order of Bank address is switched in some densities as you see in Table 1.4.

Table 1.4 Address Matching for EMRS

AHB Add	25	24	23	22	21	20	19	18	17	16	15~12	11	10	9	8	7~4	3~0	
Memory Add		BA0	BA1	12	11	10	9	8	7	6	5~2	1	0					
EMRS Setting		0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
			8				0				0	0				0	0	

Therefore, MPMC_DY_EXTENDED_MODE_REGISTER_ADDRESS_VALUE is 0x800000.

2 Configuration Table for Registers of Address Mapping, MRS and EMRS

For users' convenience, register values are shown in the tables below by every case.

2.1 MPMC_DY_CONFIG_WW_ADDRESS_MAPPING_VALUE

Table 2.1 MPMC_DY_CONFIG_WW__ADDRESS_MAPPING_VALUE

Bus	Density	Org.	Type	Row	Col	MPMC_DY_CONFIG_WW_ADDRESS_MAPPING_VALUE
16bits	64Mb	4Mx16	Mono	12	8	1280
	128Mb	8Mx16	Mono	12	9	1480
	256Mb	16Mx16	Mono	13	9	1680
	512Mb	32Mx16	Mono	13	10	1880
			DDP(1CS)	13	10	1600
1Gb	64Mx8	DDP(1CS)	13	11	1800	
32bits	64Mb	2Mx32	Mono	11	8	5300
	128Mb	4Mx32	Mono	12	8	5500
	256Mb	8Mx32	Mono	13	8	5700
	512Mb	16Mx16	DDP(1CS)	13	9	5680
	1Gb	32Mx16	DDP(1CS)	13	10	5880

*Values in the table are hexadecimal.

The value for 32-bits 512Mb (8Mx32, Mono) is not defined in Table 2.1 because it didn't exist when PL172 was designed. Since 32-bits 512Mb Mono(8Mx32) and DDP(16Mx16) have same size of bank, row and column, the value 0x5680 will allow correct operation with 32-bits 512Mb (8Mx32, Mono). However, it is not verified by ARM. It is recommended that users try PL240 or PL340 for organization of 32-bits 512Mb Mono (8Mx32).

2.2 MPMC_DY_MODE_REGISTER_ADDRESS_VALUE

Table 2.2 MPMC_DY_MODE_REGISTER_ADDRESS_VALUE

Bus	Density	Org.	Type	MPMC_DY_MODE_REGISTER_ADDRESS_VALUE											
				CL 1				CL 2				CL3			
				BL 1	BL 2	BL 4	BL 8	BL 1	BL 2	BL 4	BL 8	BL 1	BL 2	BL 4	BL 8
16bits	64Mb	4Mx16	Mono	2000	2200	2400	2600	4000	4200	4400	4600	6000	6200	6400	6600
	128Mb	8Mx16	Mono	4000	4400	4800	4C00	8000	8400	8800	8C00	C000	C400	C800	CC00
	256Mb	16Mx16	Mono	4000	4400	4800	4C00	8000	8400	8800	8C00	C000	C400	C800	CC00
	512Mb	32Mx16	Mono	8000	8800	9000	9800	10000	10800	11000	11800	18000	18800	19000	19800
		32Mx8	DDP(1CS)	8000	8800	9000	9800	10000	10800	11000	11800	18000	18800	19000	19800
1Gb	64Mx8	DDP(1CS)	10000	11000	12000	13000	20000	21000	22000	23000	30000	31000	32000	33000	
32bits	64Mb	2Mx32	Mono	4000	4400	4800	4C00	8000	8400	8800	8C00	C000	C400	C800	CC00
	128Mb	4Mx32	Mono	4000	4400	4800	4C00	8000	8400	8800	8C00	C000	C400	C800	CC00
	256Mb	8Mx32	Mono	4000	4400	4800	4C00	8000	8400	8800	8C00	C000	C400	C800	CC00
	512Mb	16Mx16	DDP(1CS)	8000	8800	9000	9800	10000	10800	11000	11800	18000	18800	19000	19800
	1Gb	32Mx16	DDP(1CS)	10000	11000	12000	13000	20000	21000	22000	23000	30000	31000	32000	33000

*Values in the table are hexadecimal.

2.3 MPMC_DY_EXTENDED_MODE_REGISTER_ADDRESS_VALUE

Table 2.3 MPMC_DY_EXTENDED_MODE_REGISTER_ADDRESS _ VALUE

Bus	Density	Org.	Type	MPMC_DY_EXTENDED_MODE_REGISTER_ADDRESS_VALUE											
				PASR Full				PASR 1/2				PASR 1/4			
				DS Full	DS 1/2	DS 1/4	DS 1/8	DS Full	DS 1/2	DS 1/4	DS 1/8	DS Full	DS 1/2	DS 1/4	DS 1/8
16bits	64Mb	4Mx16	Mono	200000	204000	208000	20C000	200200	204200	208200	20C200	200400	204400	208400	20C400
	128Mb	8Mx16	Mono	800000	808000	810000	818000	800400	808400	810400	818400	800800	808800	810800	818800
	256Mb	16Mx16	Mono	800000	808000	810000	818000	800400	808400	810400	818400	800800	808800	810800	818800
	512Mb	32Mx16	Mono	2000000	2010000	2020000	2030000	2000800	2010800	2020800	2030800	2001000	2011000	2021000	2031000
		32Mx8	DDP(1CS)	2000000	2010000	2020000	2030000	2000800	2010800	2020800	2030800	2001000	2011000	2021000	2031000
1Gb	64Mx8	DDP(1CS)	4000000	4020000	4040000	4060000	4001000	4021000	4041000	4061000	4002000	4022000	4042000	4062000	
32bits	64Mb	2Mx32	Mono	200000	208000	210000	218000	200400	208400	210400	218400	200800	208800	210800	218800
	128Mb	4Mx32	Mono	800000	808000	810000	818000	800400	808400	810400	818400	800800	808800	810800	818800
	256Mb	8Mx32	Mono	800000	810000	820000	830000	800800	810800	820800	830800	801000	811000	821000	831000
	512Mb	16Mx16	DDP(1CS)	2000000	2010000	2020000	2030000	2000800	2010800	2020800	2030800	2001000	2011000	2021000	2031000
	1Gb	32Mx16	DDP(1CS)	2000000	2020000	2040000	2060000	2001000	2021000	2041000	2061000	2002000	2022000	2042000	2062000

*Values in the table are hexadecimal.